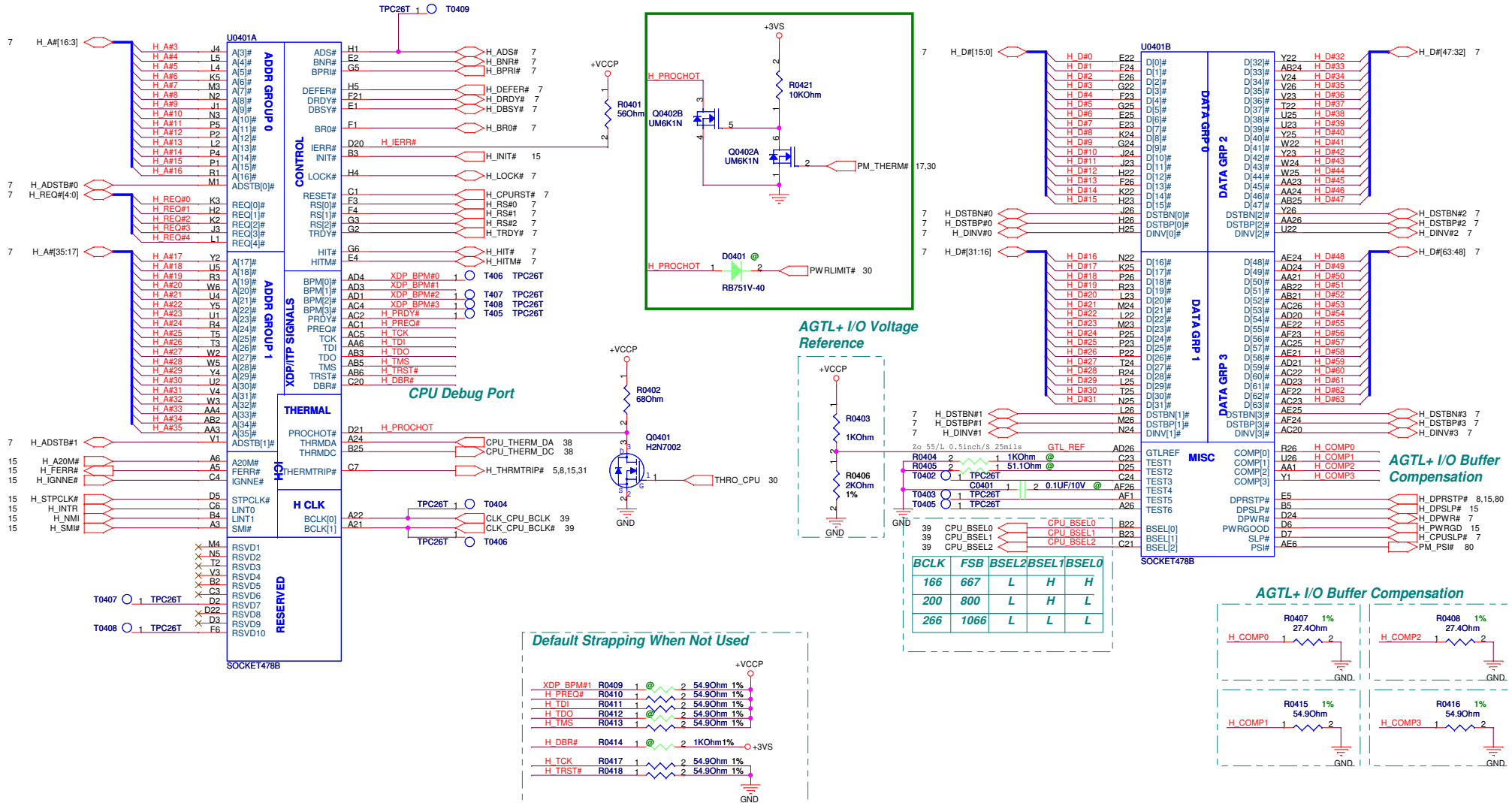
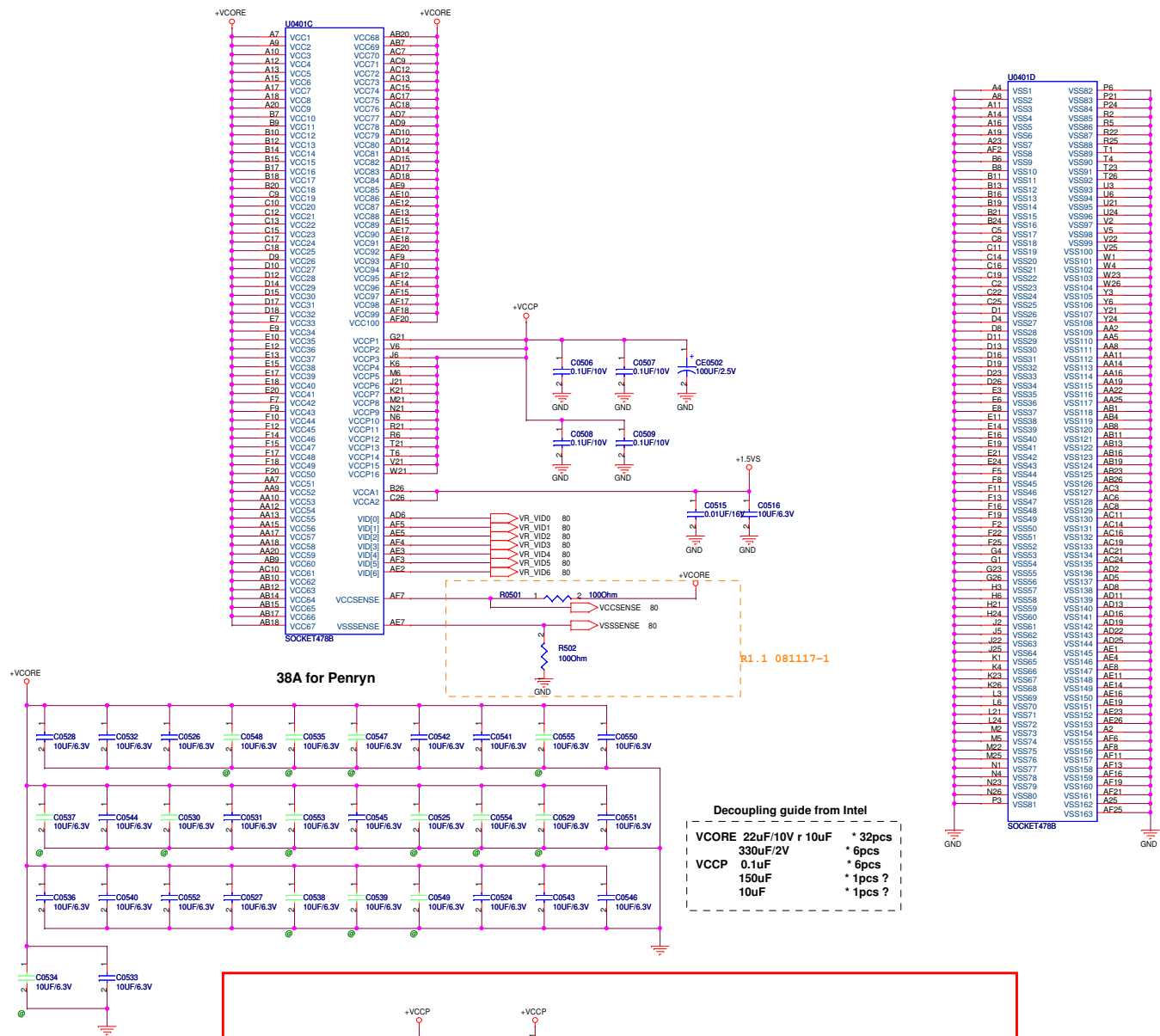


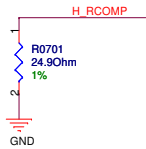
add test point





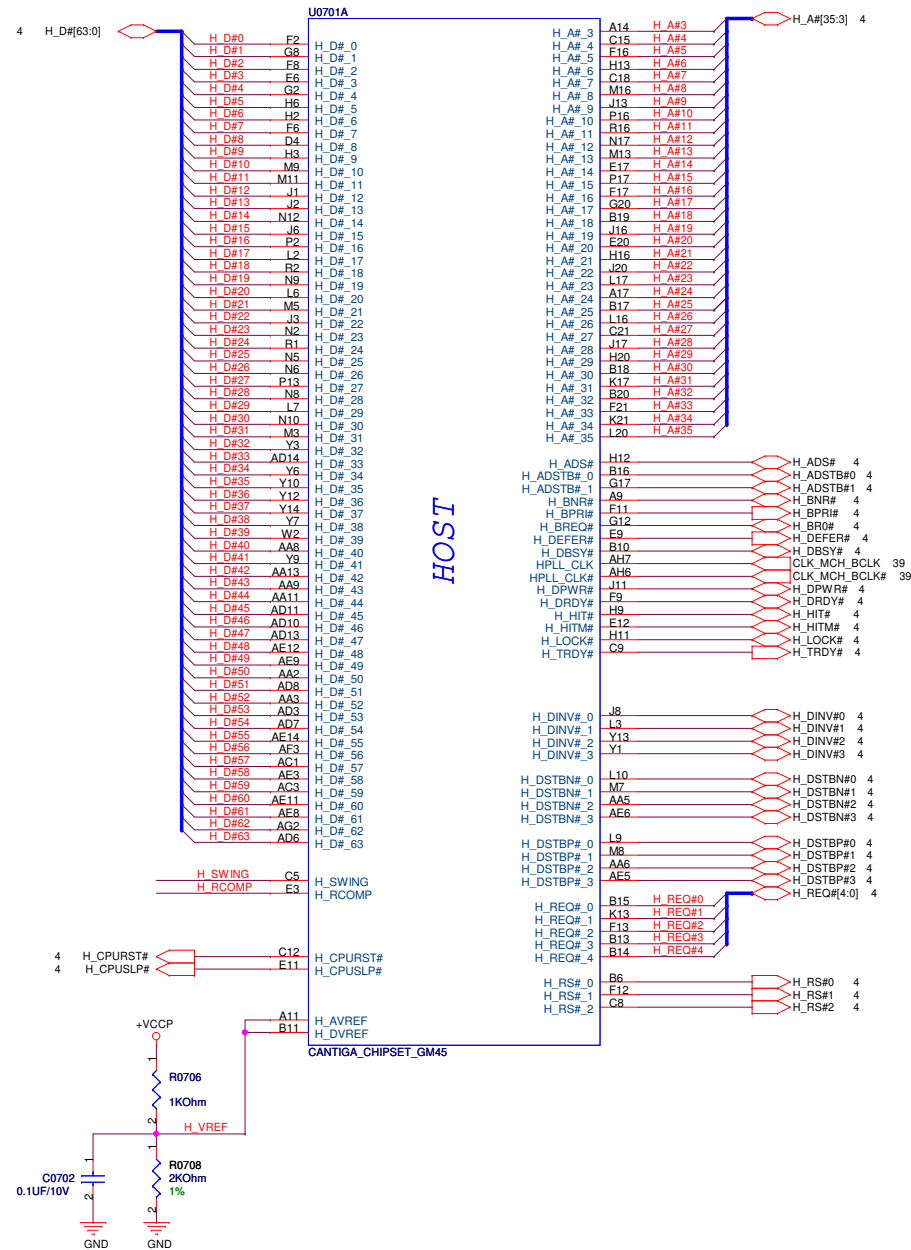
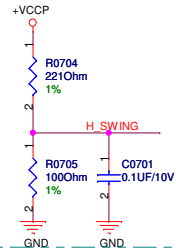
RCOMP

For Calibrating the FSB I/O Buffer

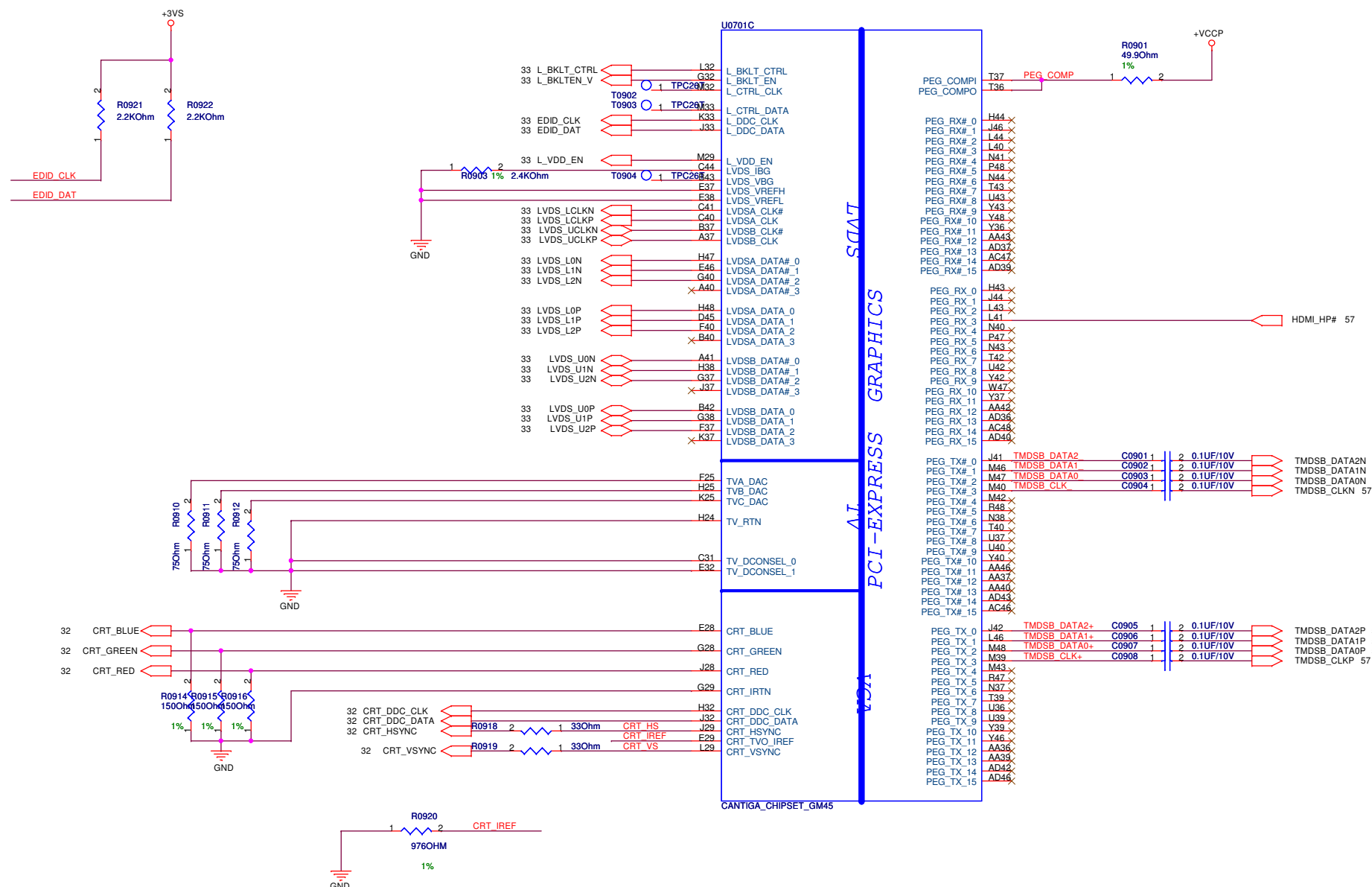


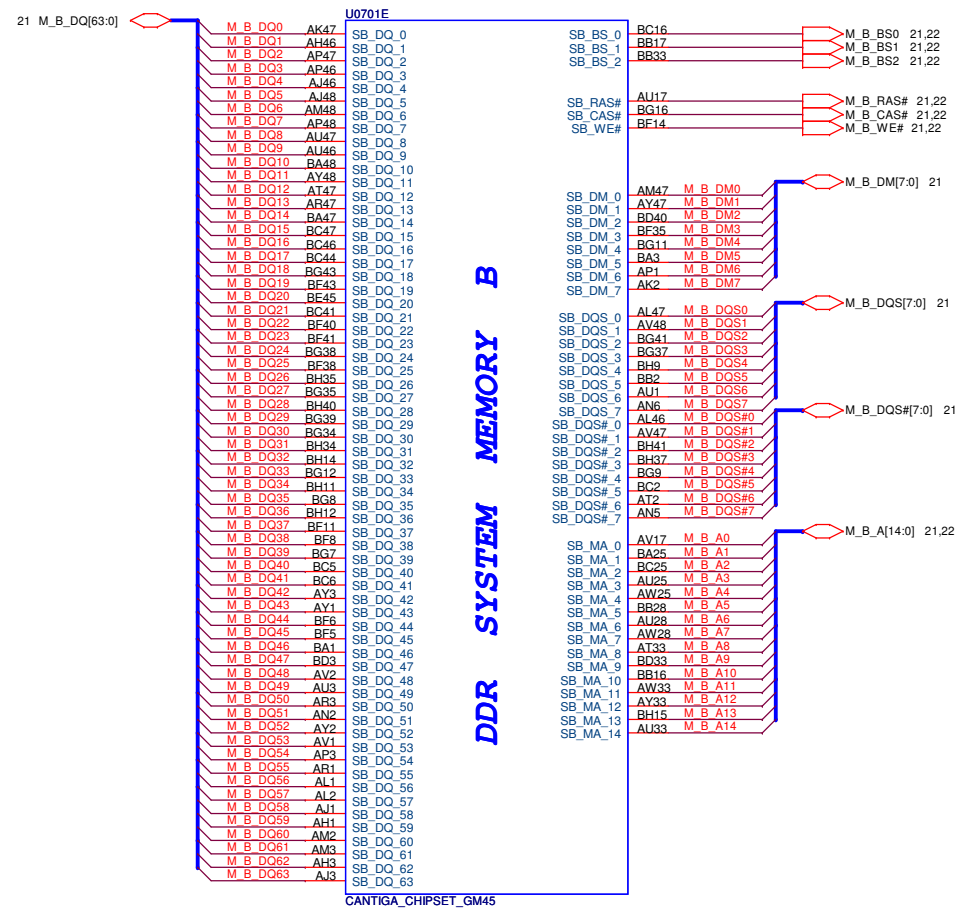
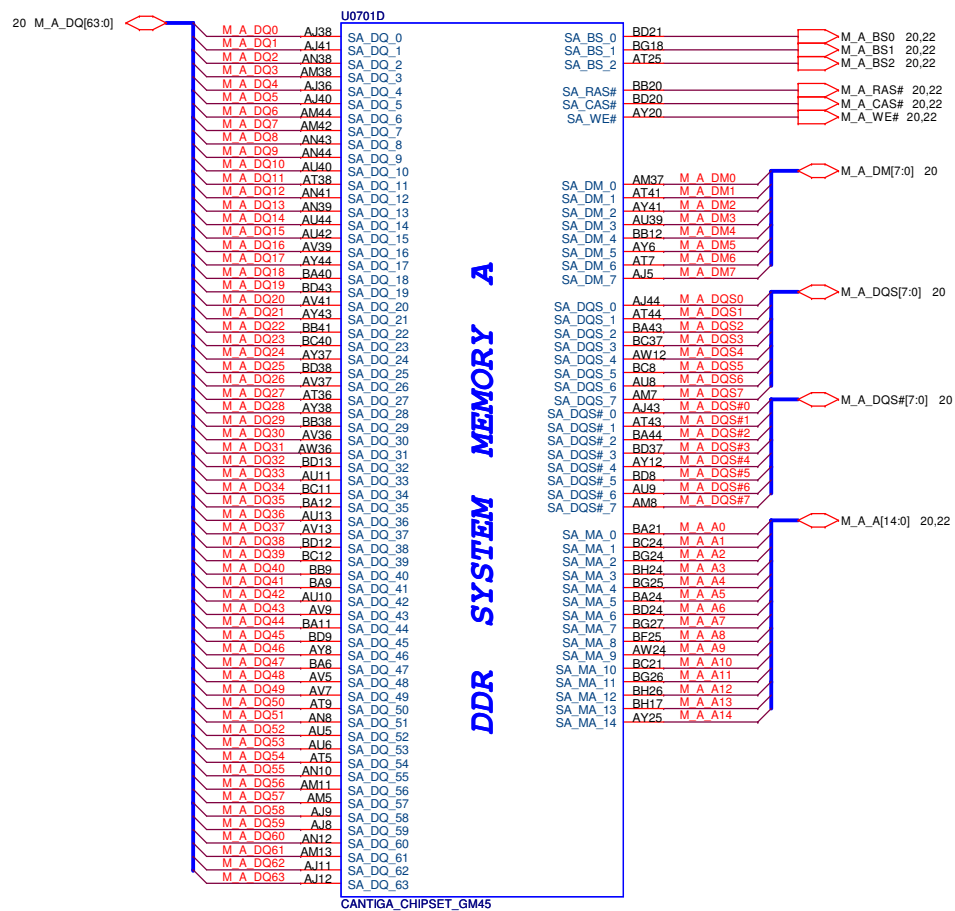
Voltage Swing

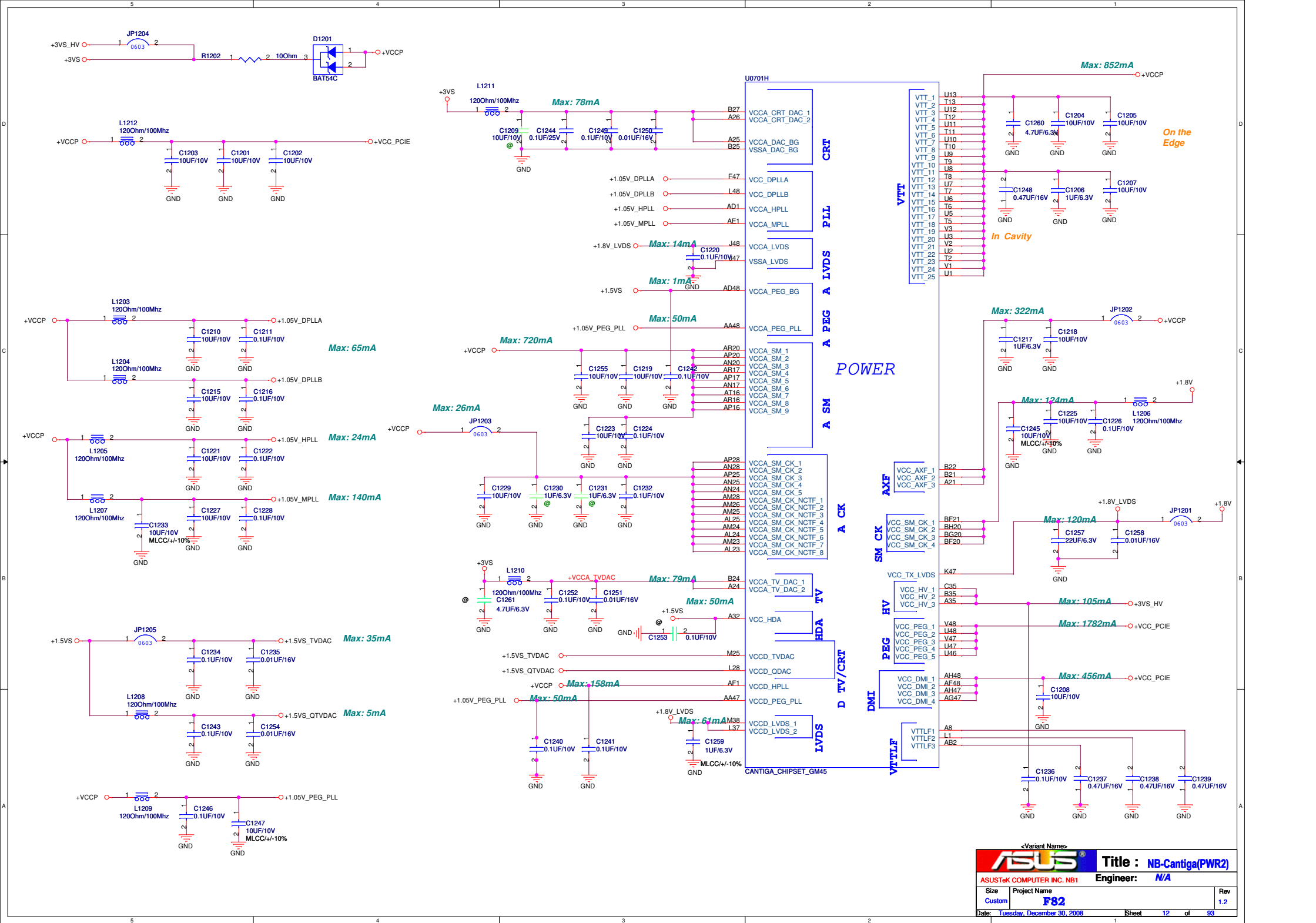
For Providing a Reference Voltage to The FSB RCOMP circuits

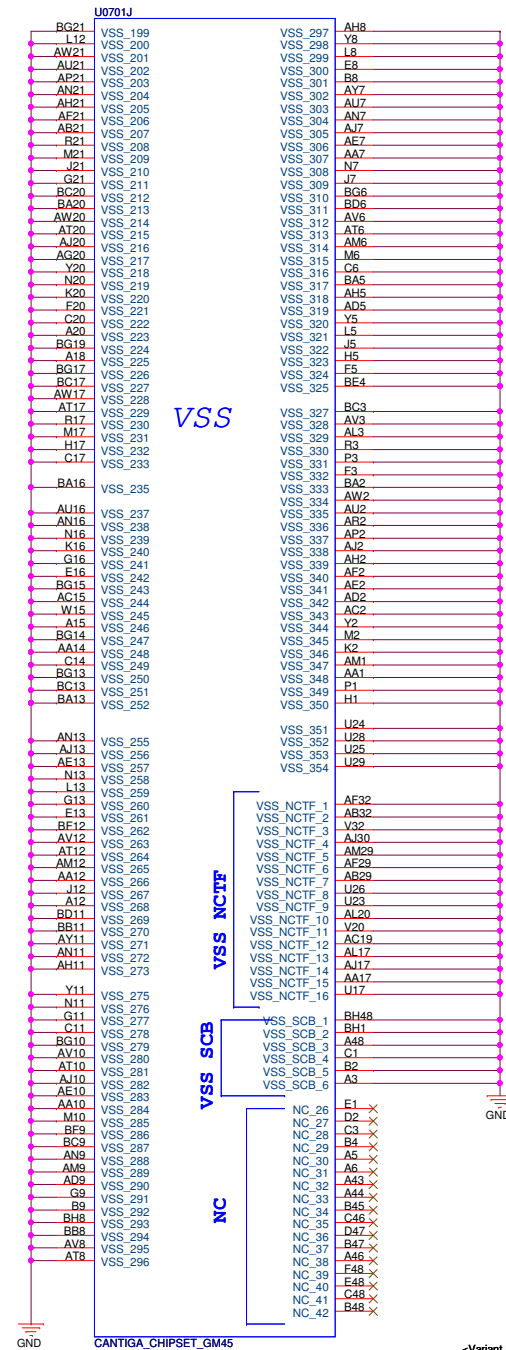
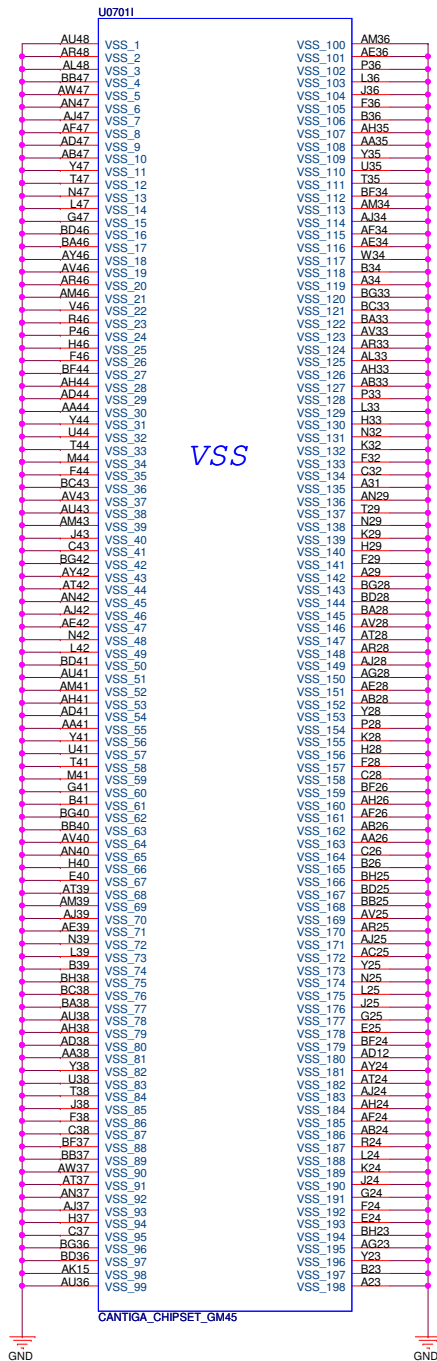


<Variant Name>

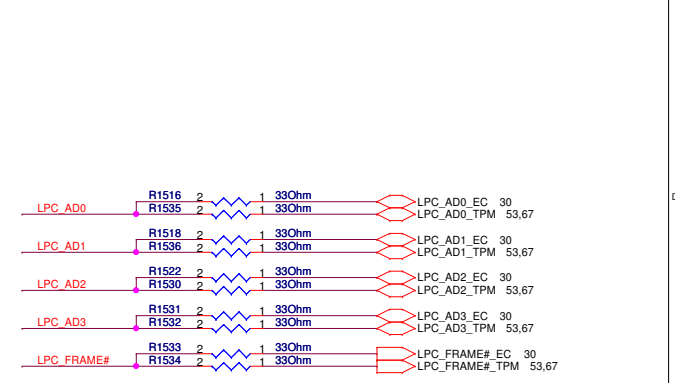
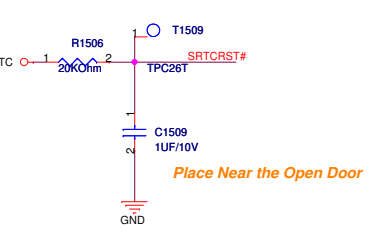
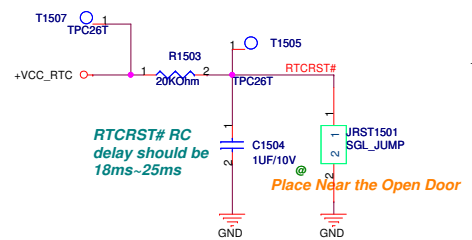
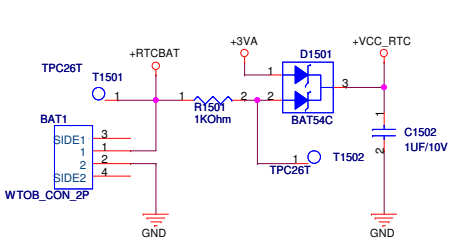




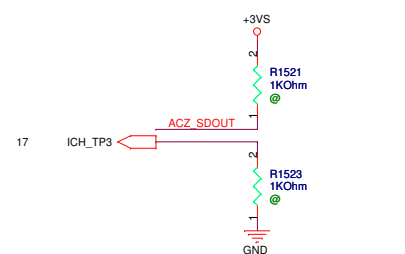




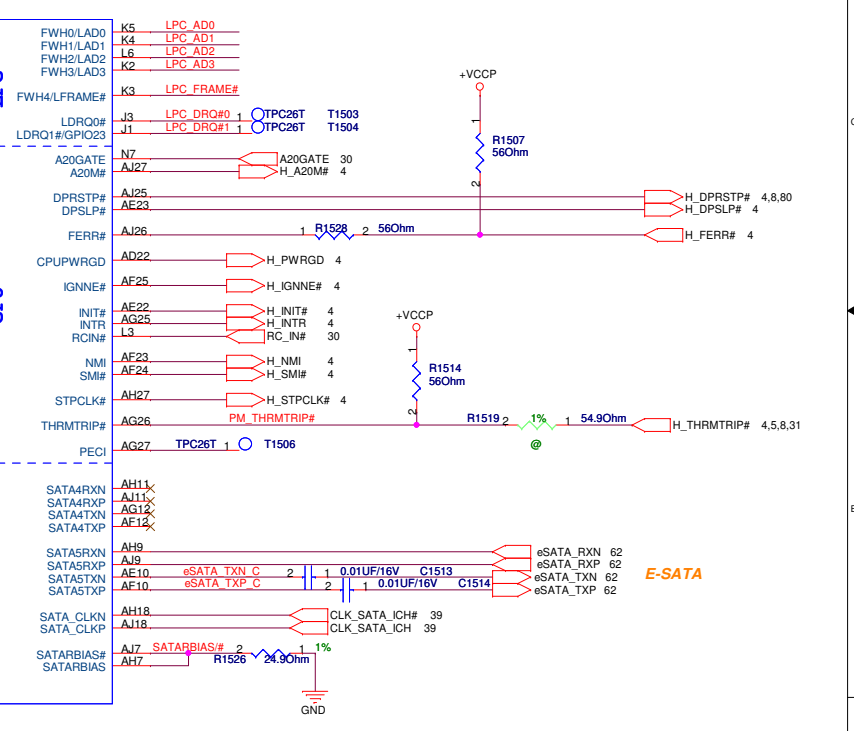
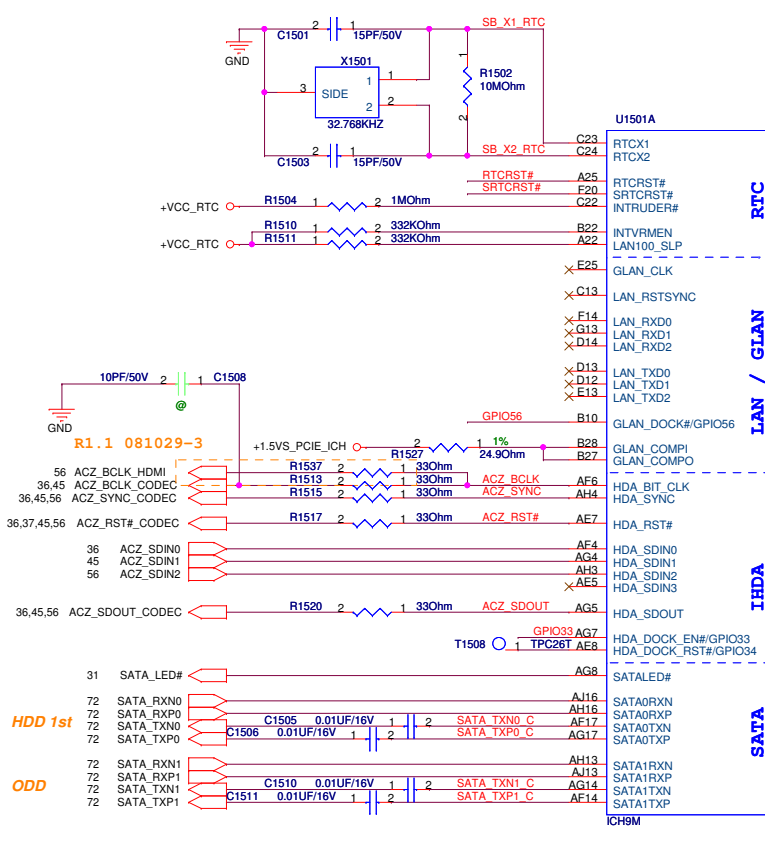
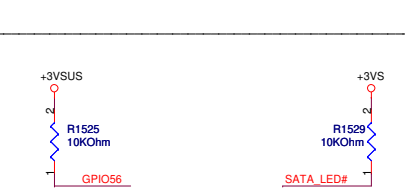
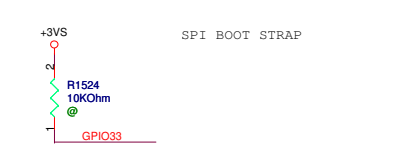
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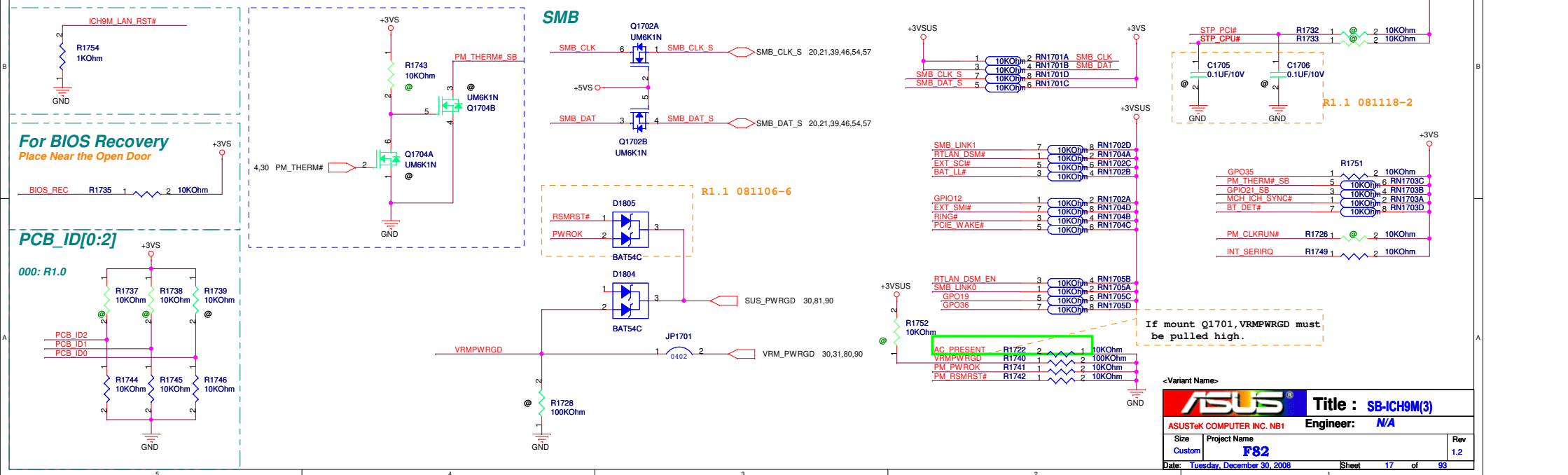


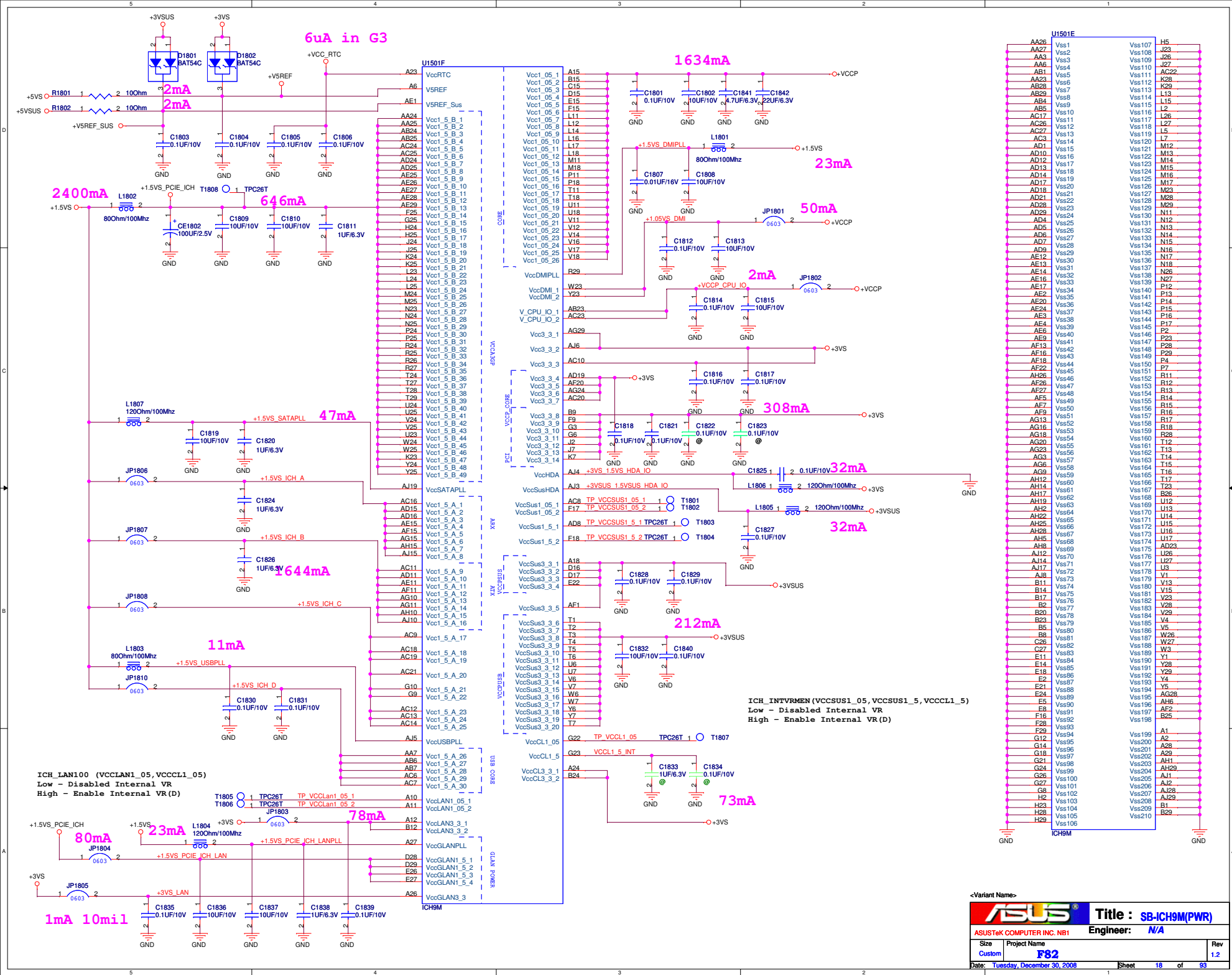
ICH_INTVRMEN(VCCSUS1_05,VCCSUS1_5,VCCCL1_5)
Low - Disabled Internal VR
High - Enable Internal VR(D)
ICH_LAN100(VCCLAN1_05,VCCCL1_05)
Low - Disabled Internal VR
High - Enable Internal VR(D)



ICH_TP3	ACZ_SDOUT	Description
0	0	RSVD
1	1	Enter XOR Chain
0	0	Normal Operation (D)
1	1	Set PCIe port config bit 1

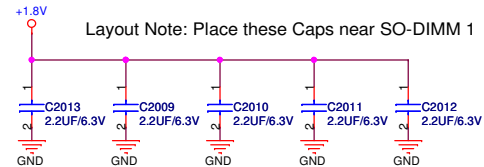
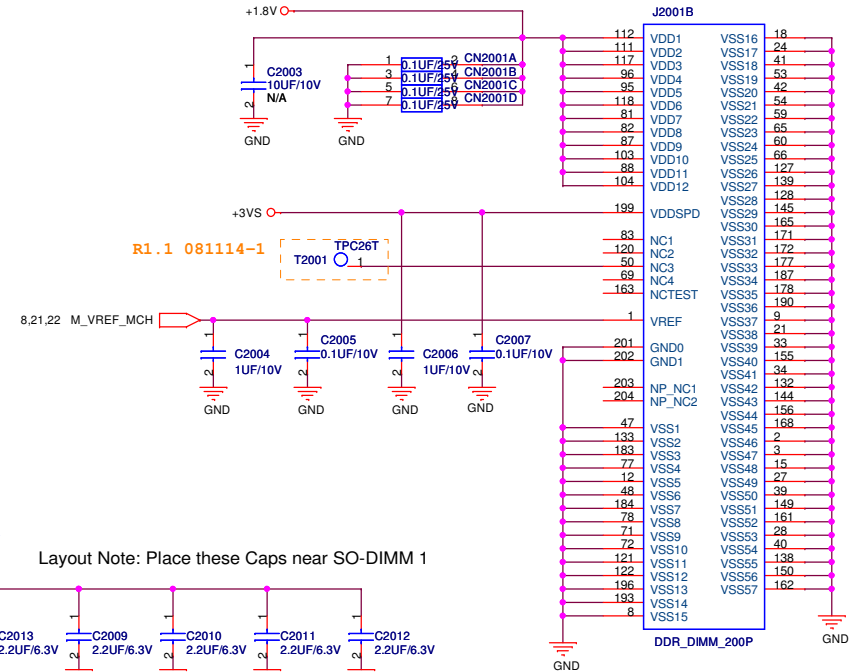
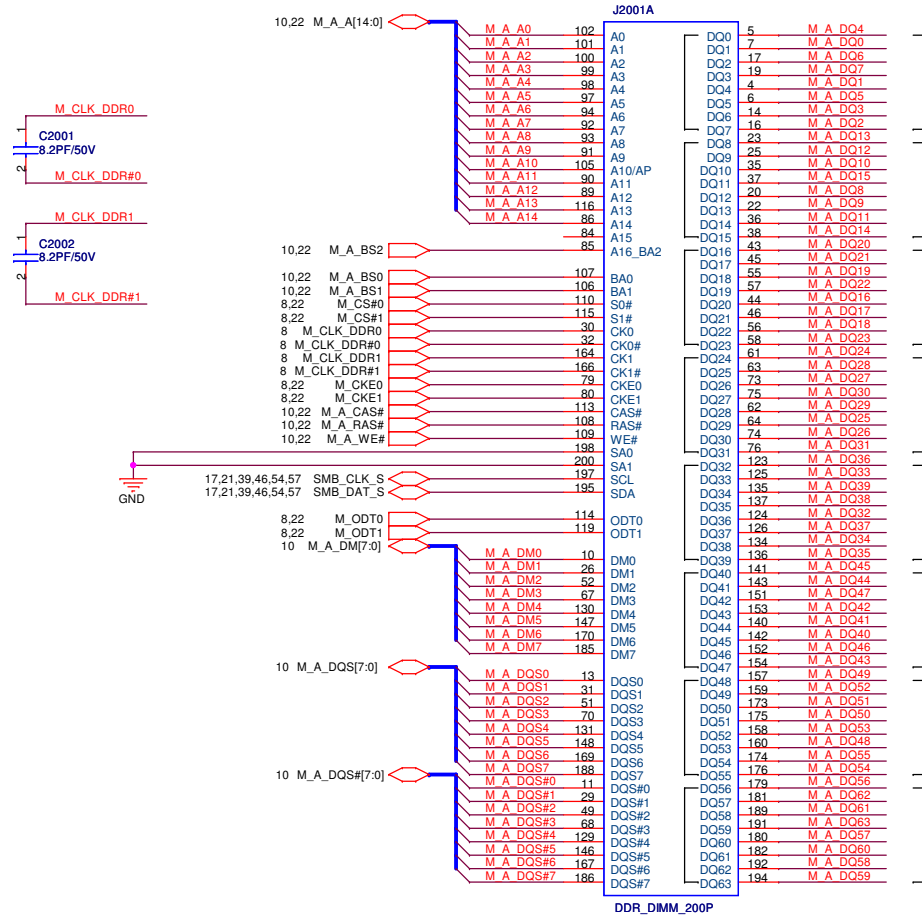




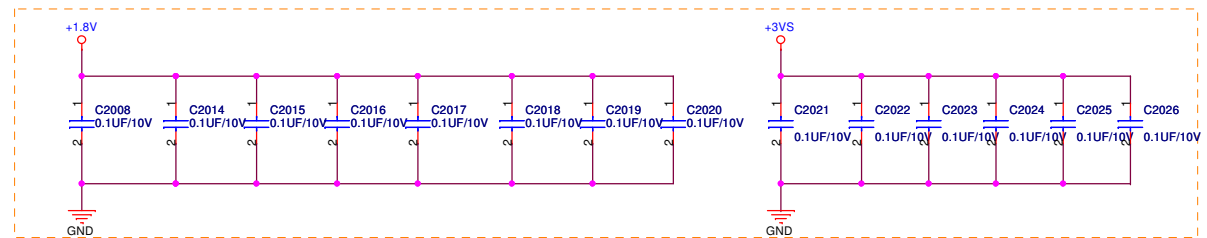


DDR2 200P H=4.0mm (Reverse Type)

M_A_DQ[63:0] 10

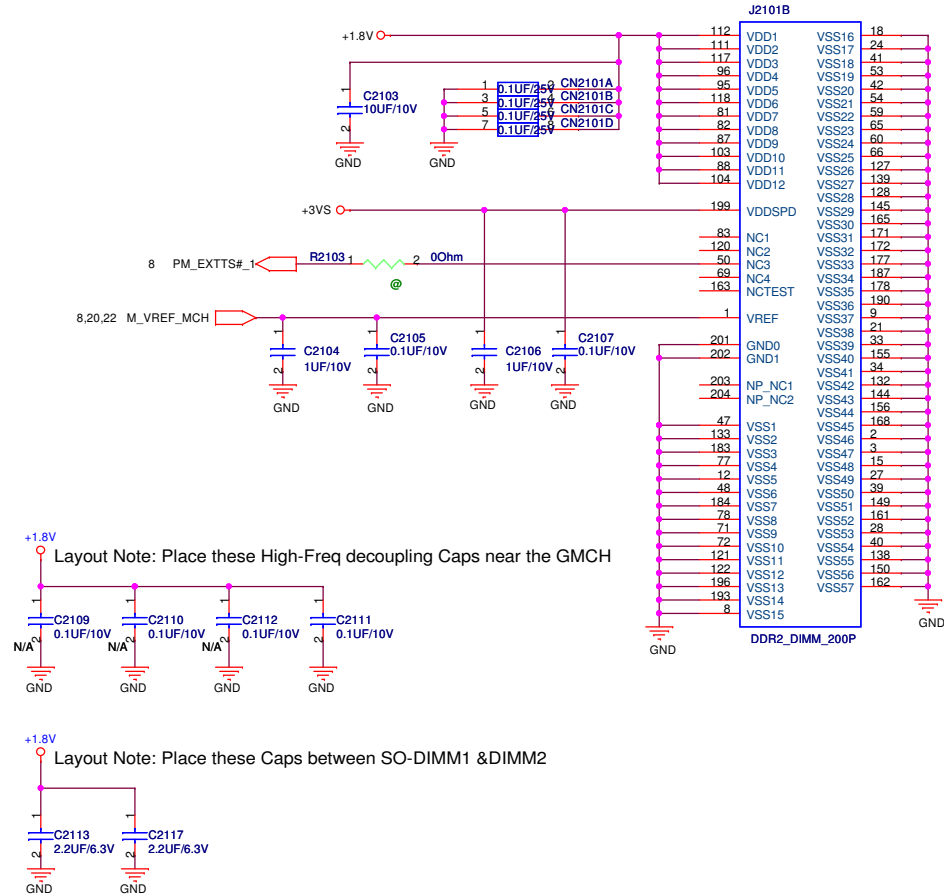
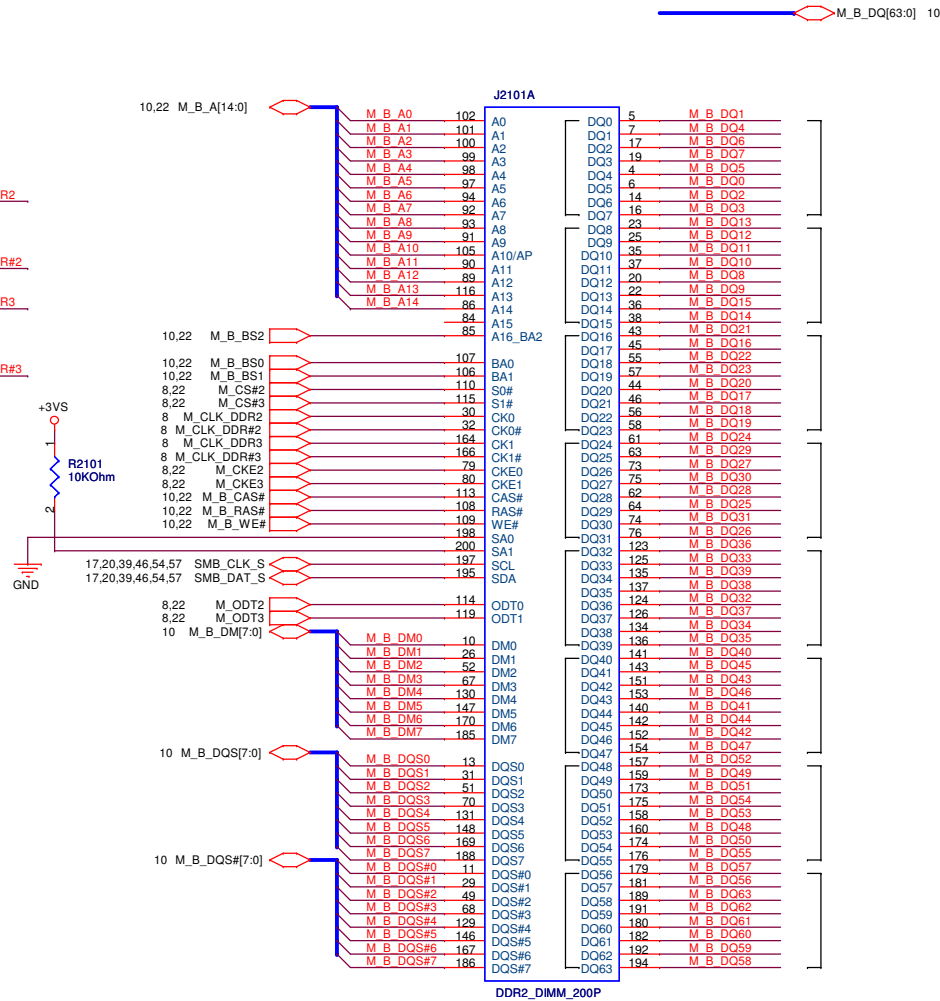


R1.1 081114-2 For EMI request.



<Variant Name>

DDR2 200P H=9.2mm (Reverse Type)



<Variant Name>



10,20 M_A_A[13:0]
10,21 M_B_A[13:0]

8,20 M_ODT1
8,20 M_CS#0
8,20 M_ODT0
10,20 M_A_RAS#
10,20 M_A_BS1
8,20 M_CS#1
10,20 M_A_WE#

10,20 M_A_A14
10,20 M_A_BS0

8,20 M_CKE1

10,20 M_A_BS2
8,20 M_CKE0

10,20 M_A_CAS#

10,21 M_B_A14

10,21 M_B_BS1

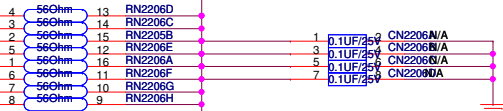
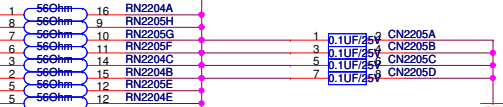
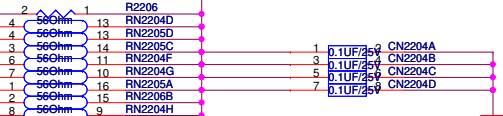
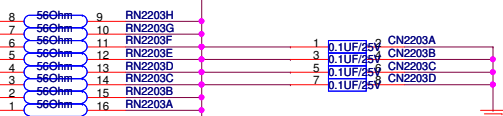
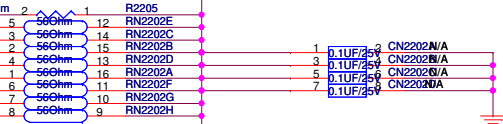
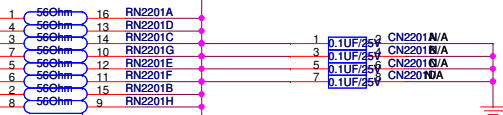
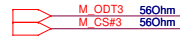
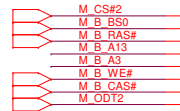
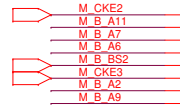
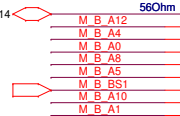
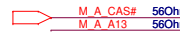
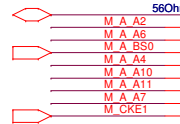
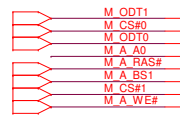
8,21 M_CKE2

10,21 M_B_BS2
8,21 M_CKE3

8,21 M_CS#2
10,21 M_B_BS0
10,21 M_B_RAS#

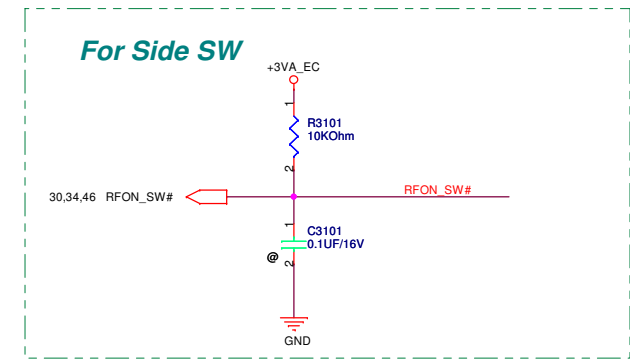
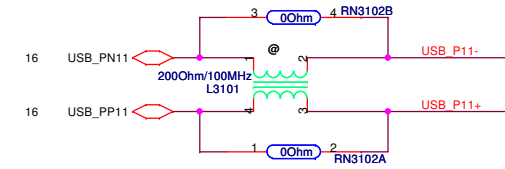
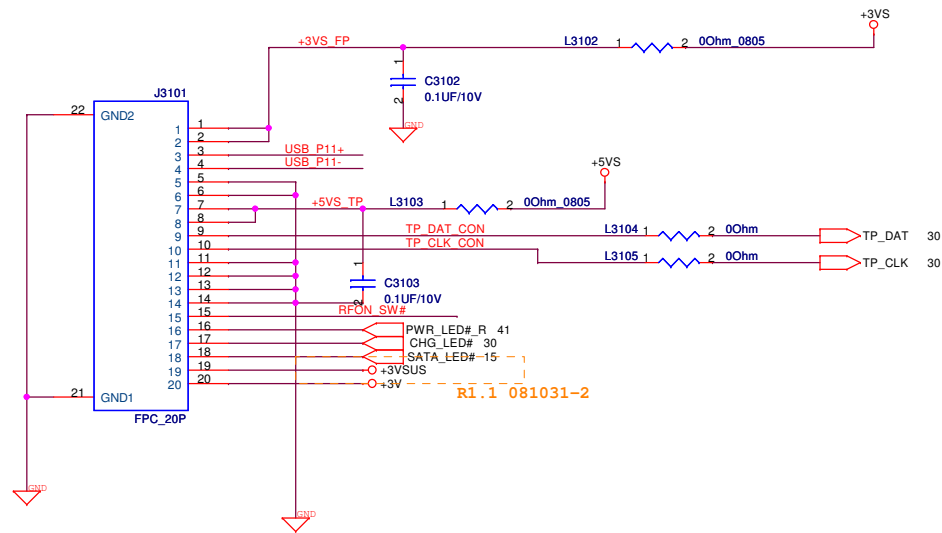
10,21 M_B_WE#
10,21 M_B_CAS#
8,21 M_ODT2

8,21 M_ODT3
8,21 M_CS#3

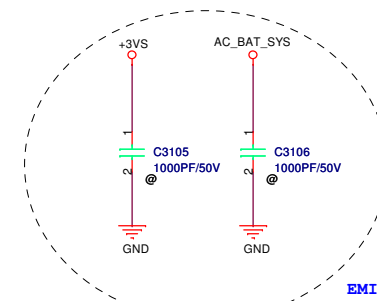
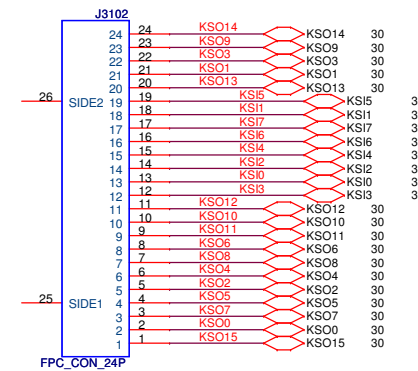


<Variant Name>

TouchPad & FingerPrint

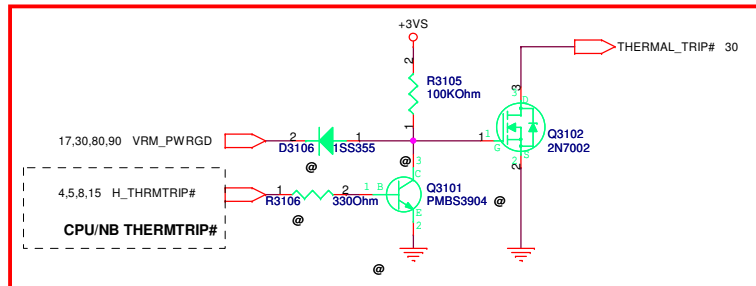


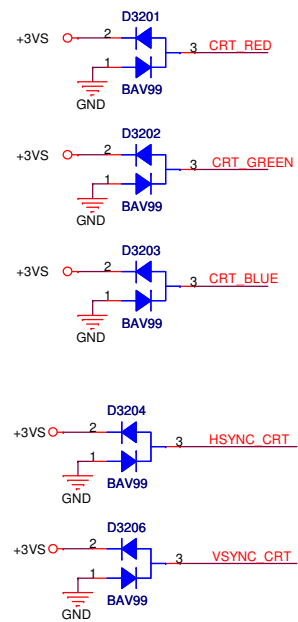
Keyboard Connector



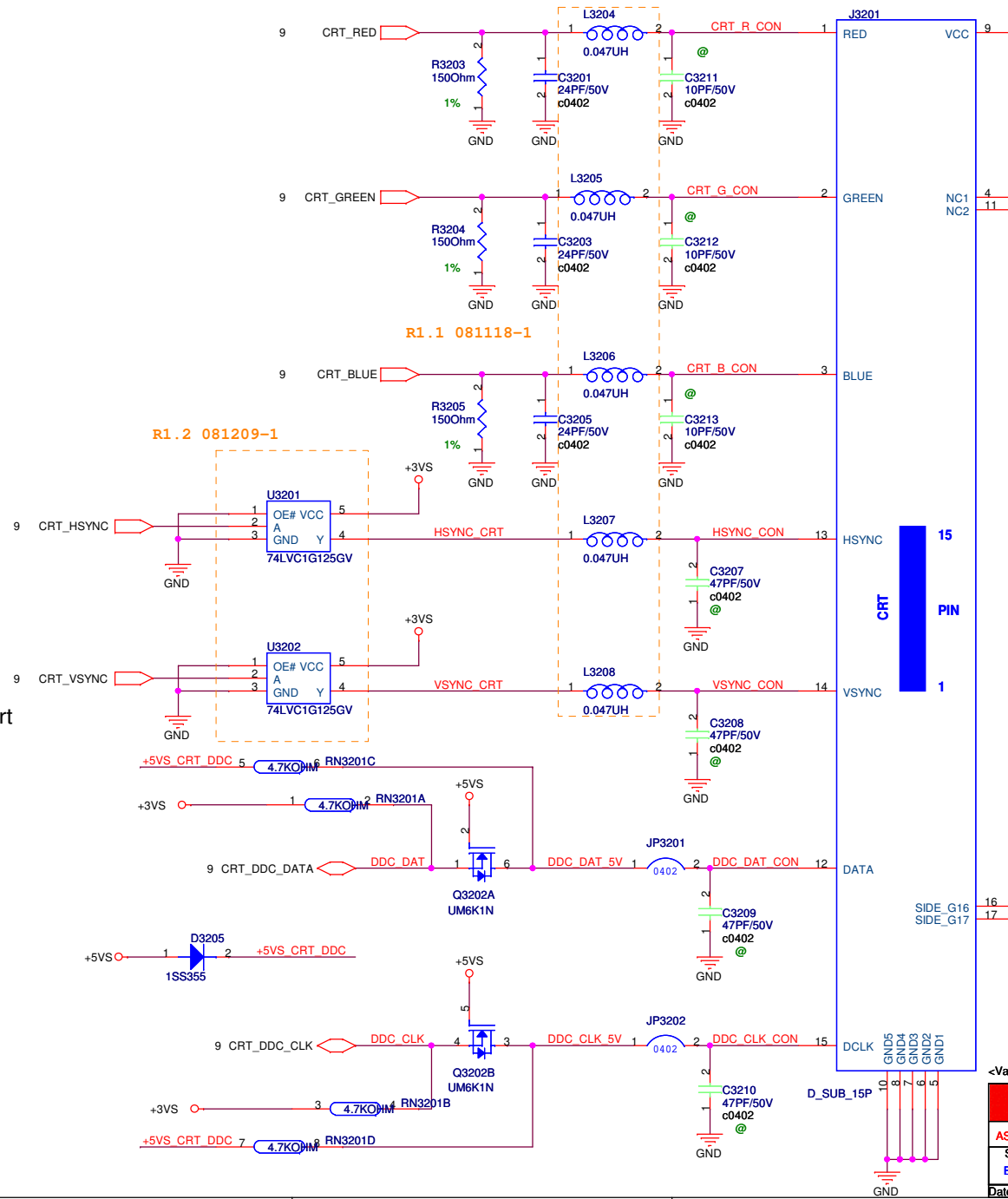
For Thermal Control Method

Remove redundant components





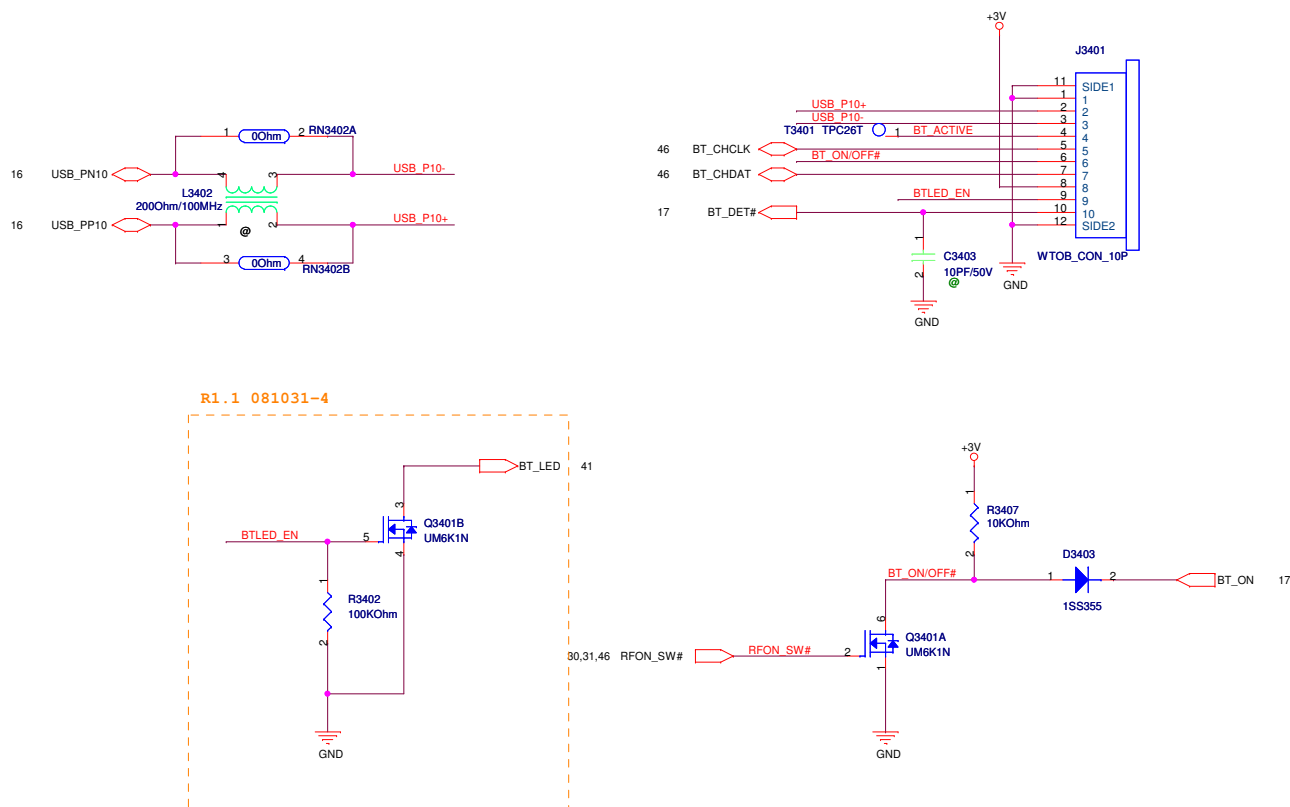
PLACE ESD Diodes near VGA port



<Variant Name>

ASUS		Title : CRT	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size B	Project Name F82	Rev 1.2	
Date: Tuesday, December 30, 2008		Sheet 32 of 93	

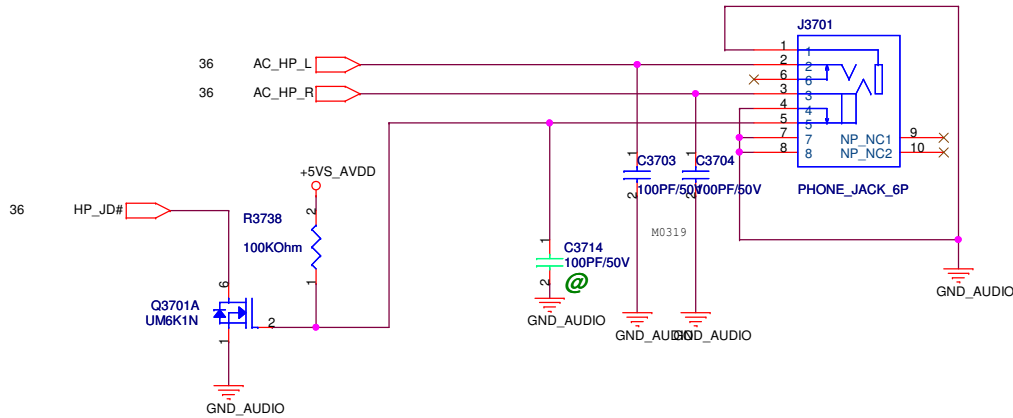
For Bluetooth



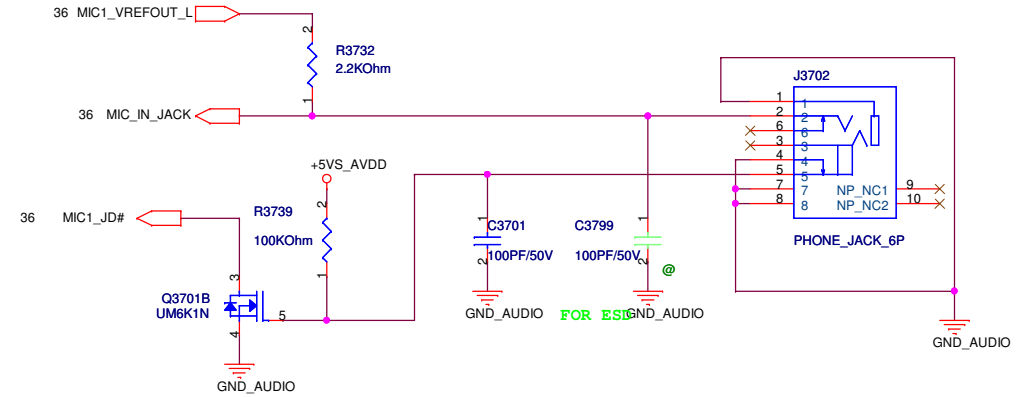
<Variant Name>

ASUS		Title : BT	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	F82	1.2	
Date: Tuesday, December 30, 2008		Sheet	34 of 93

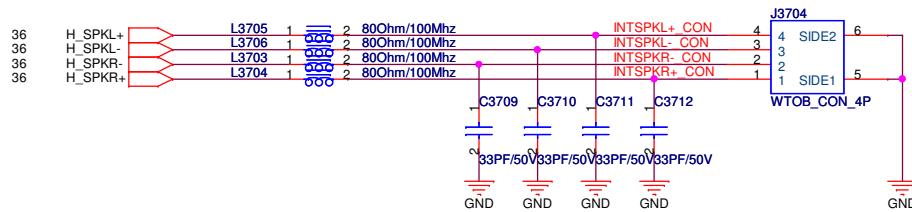
HP CONN



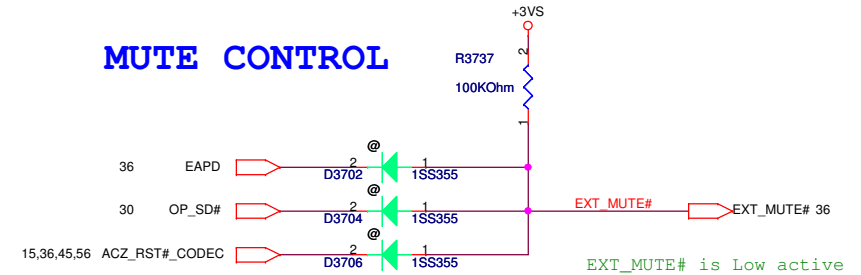
External MIC CONN



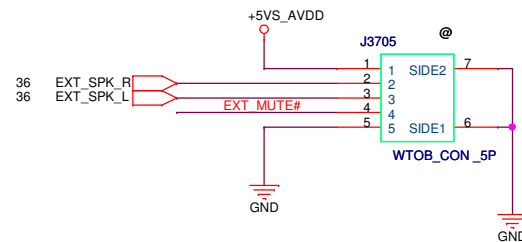
SPEAKER CONNECTOR (2W)



MUTE CONTROL

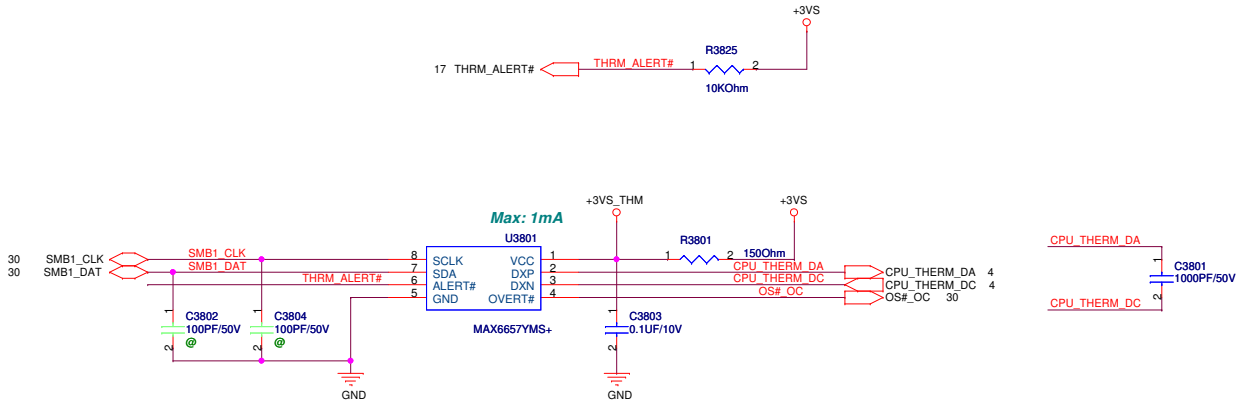


EXTENSION SPEAKER CONNECTOR

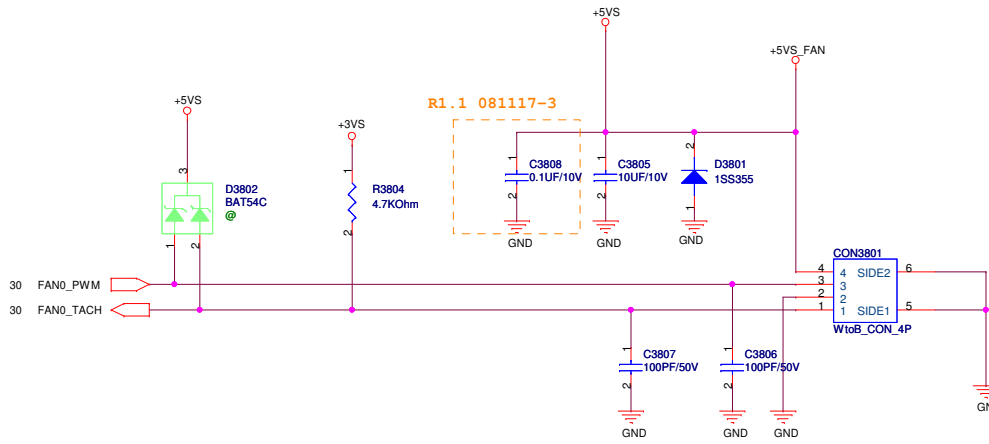


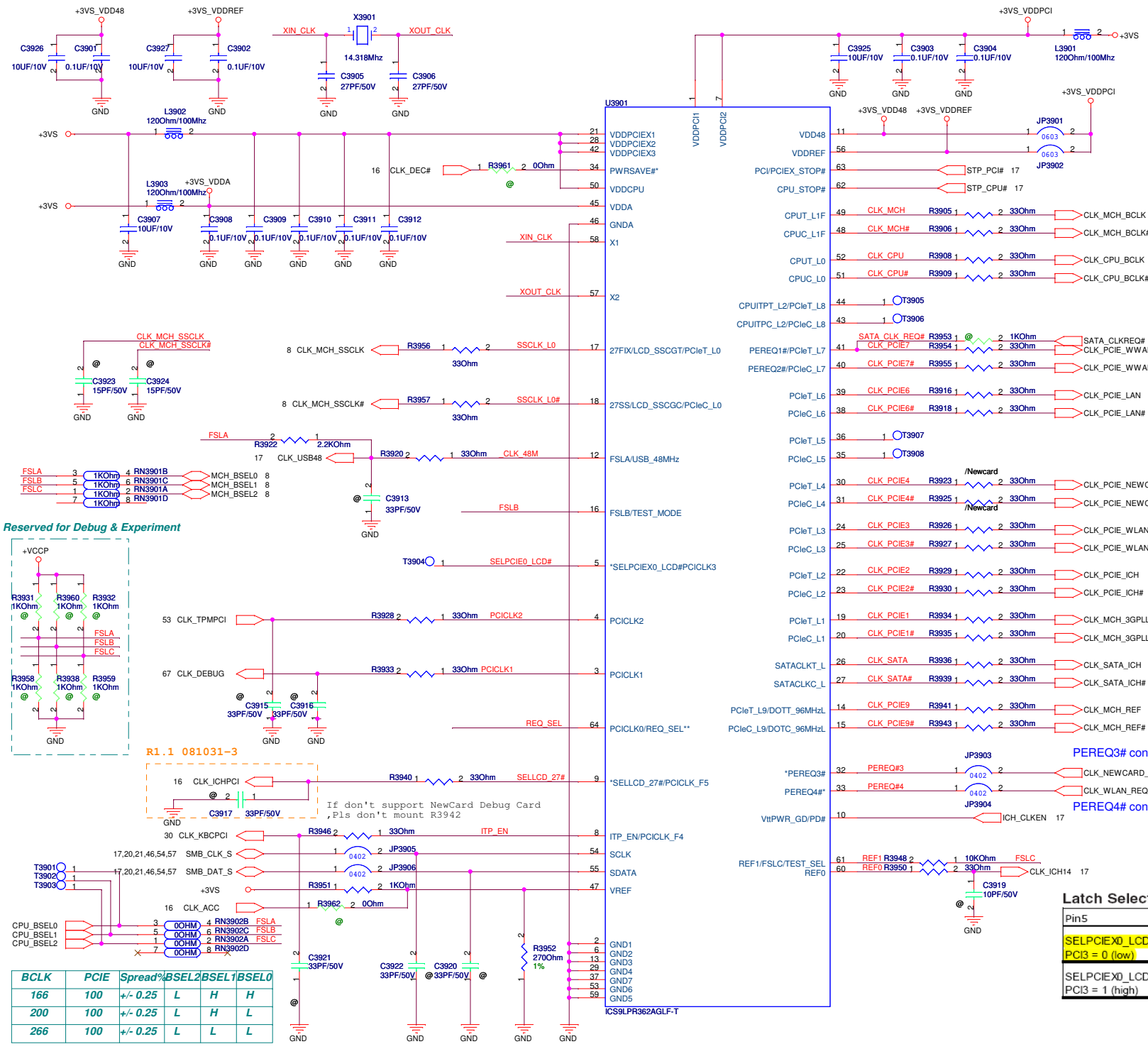
ASUS		Title : AUDIO HP/MIC	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size B	Project Name F82	Date: Tuesday, December 30, 2008	Rev 1.2
Sheet 37 of 93			

Thermal Sensor



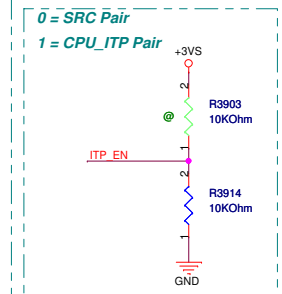
add 2nd source :06G023096010



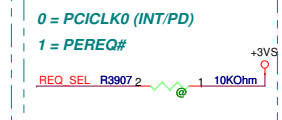


Latched Input Select

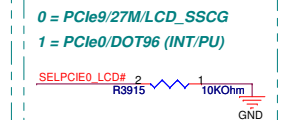
ITP_EN/PCICLK_F4



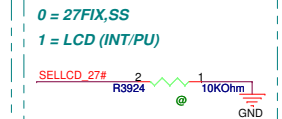
PCICLK0/REQ_SEL



SELPCIE0_LCD#PCICLK3



SELLCD_27#/PCICLK_F5



Latch Select Table

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE0_LCD# PC3 = 0 (low)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE9 DOT96	27FIX/SS LCD
SELPCIE0_LCD# PC3 = 1 (high)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE9 DOT96	PCIE9 PCIE9

<Variant Name>

Title :CLOCK GEN-4CS9LPR363

ASUSTek COMPUTER INC. NBI

Engineer: N/A

Size Custom

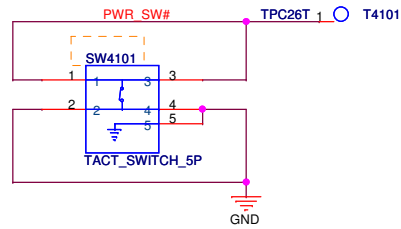
Project Name F82

Date: Tuesday, December 30, 2008

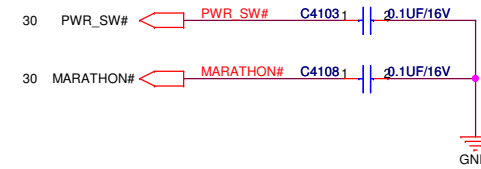
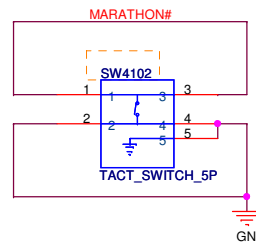
Sheet 39 of 93

Rev 1.2

SWITCH BUTTON

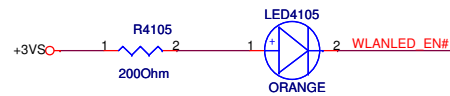


R1.1 081106-1

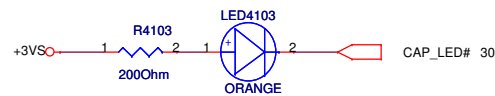


LED

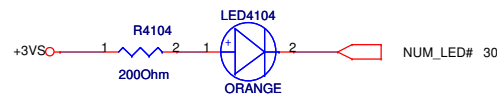
For WireLess LED



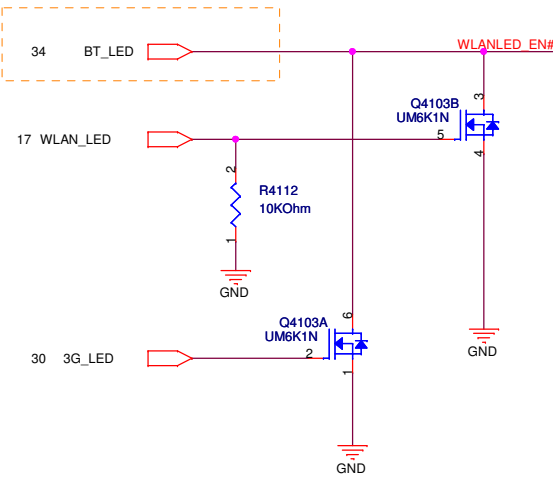
for Cap. Lock



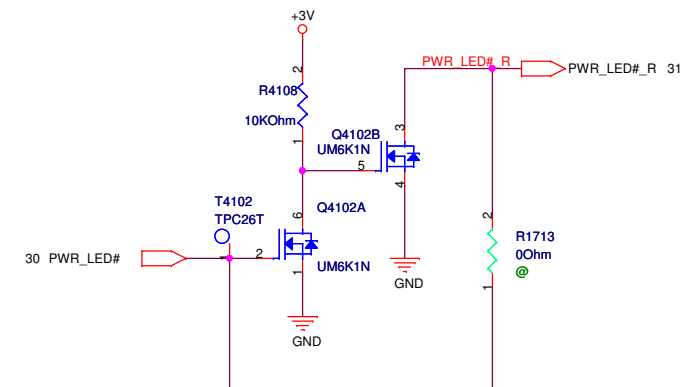
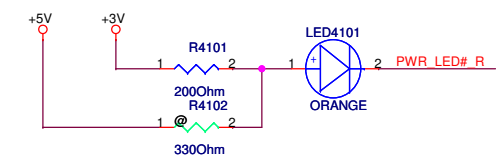
for Num Lock



R1.1 081031-4



For POWER LED



<Variant Name>



Title : Switch Button & LED

ASUSTeK COMPUTER INC

Engineer: *N/A*

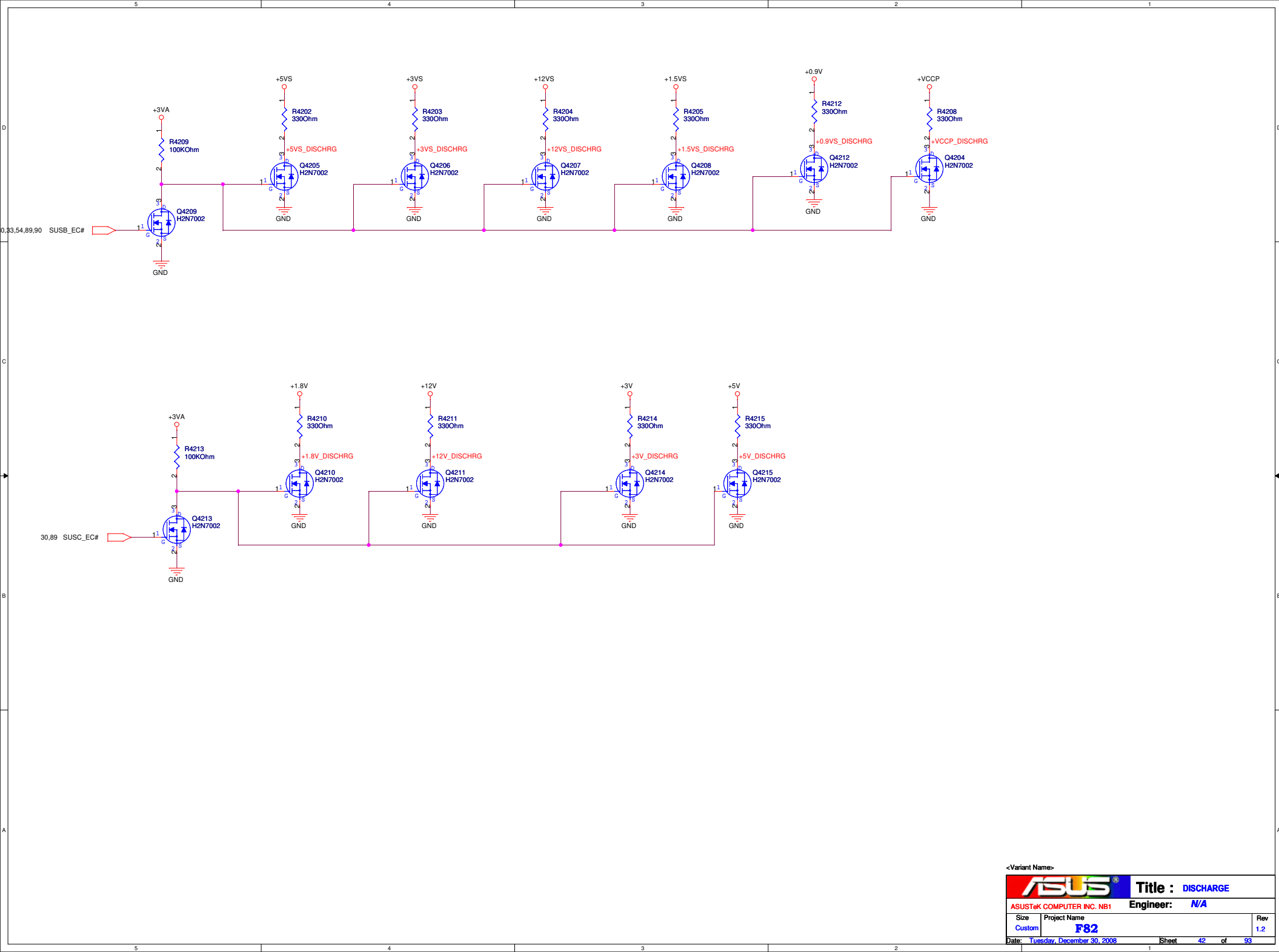
Size B	Project Name F8
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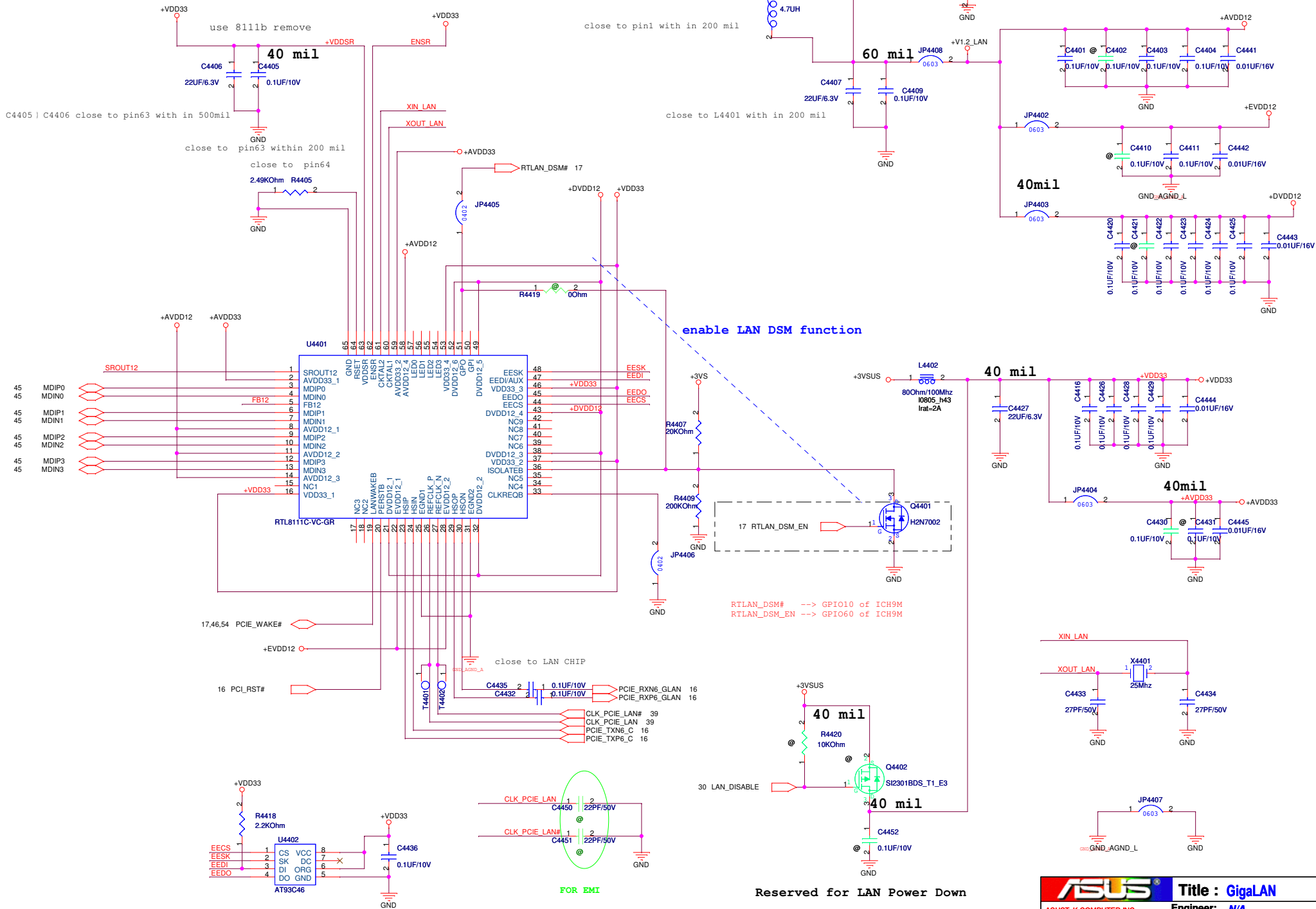
Project Name	F82
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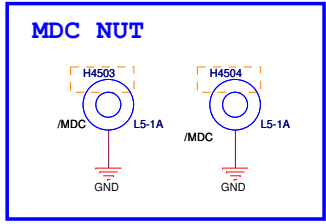
Rev	
1.2	

Date: Tuesday, December 30, 2008

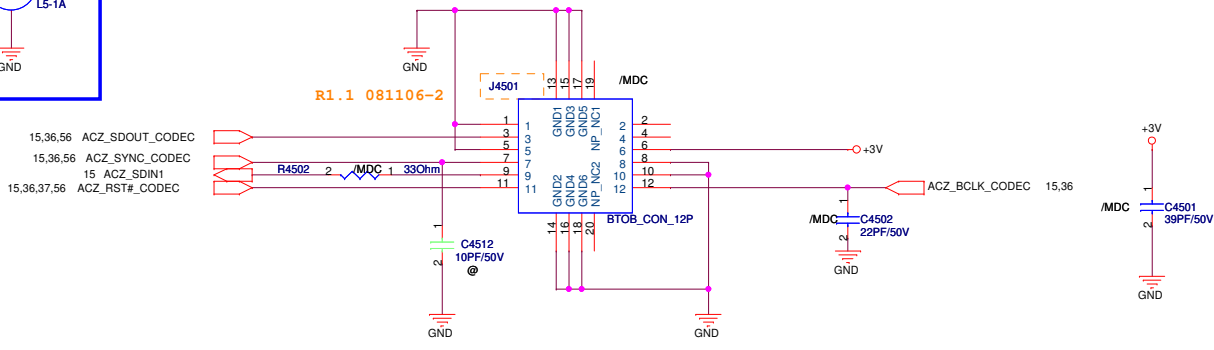
Sheet 41 of 93



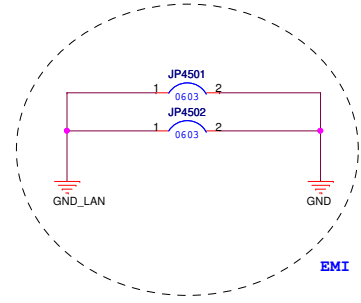
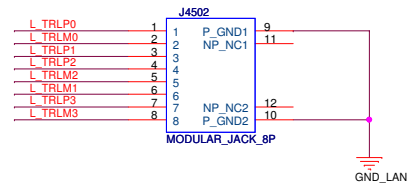
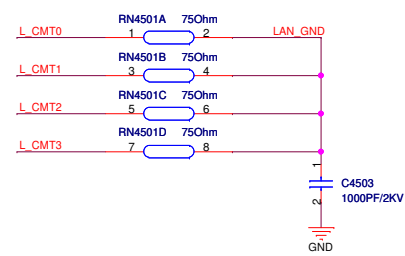
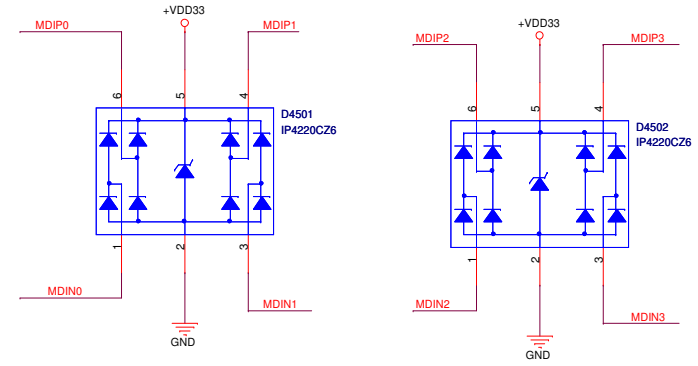
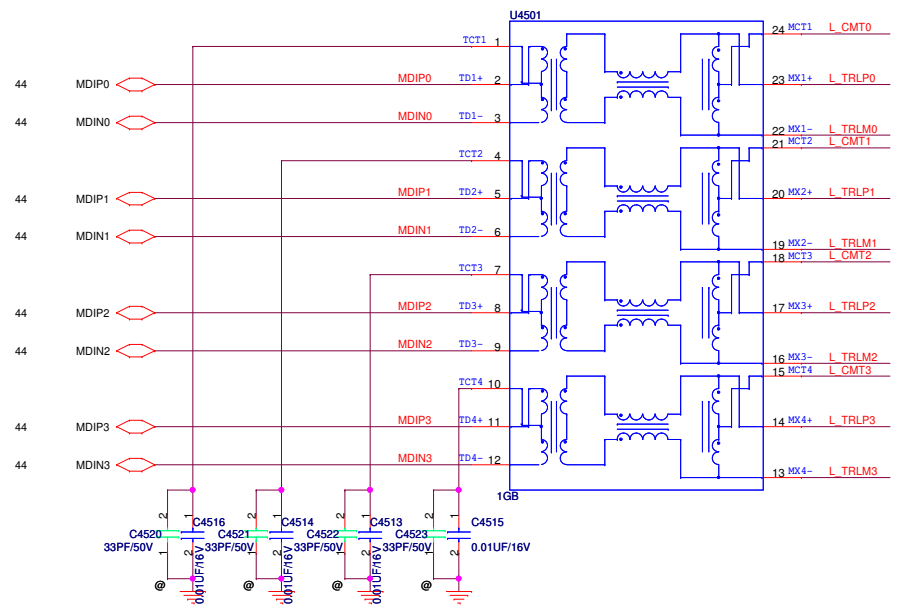


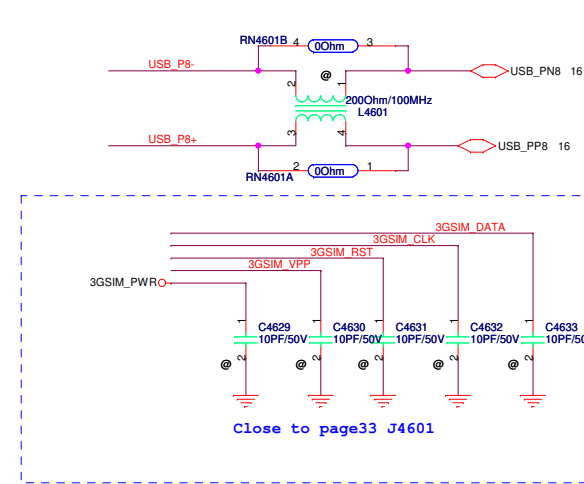
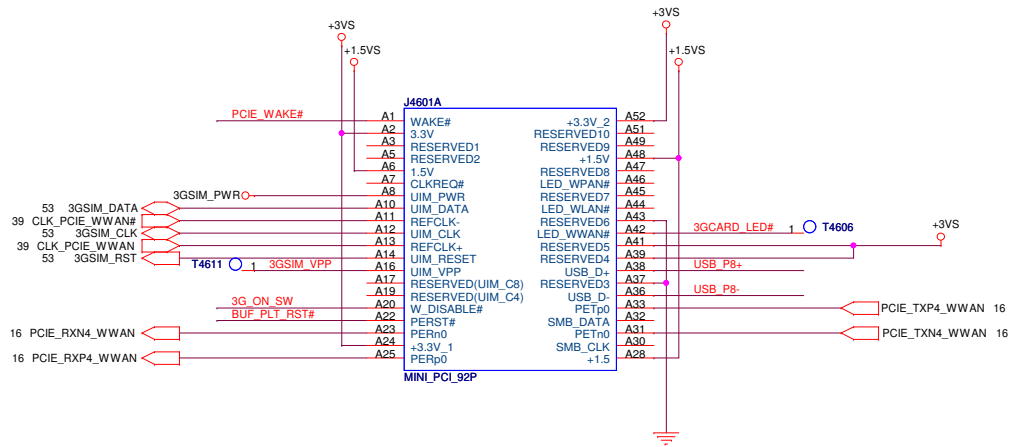


MDC CONN.

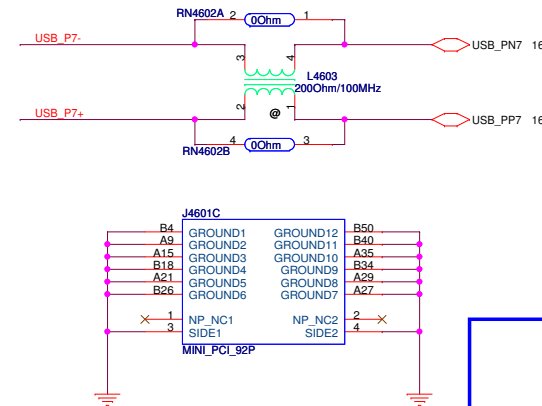
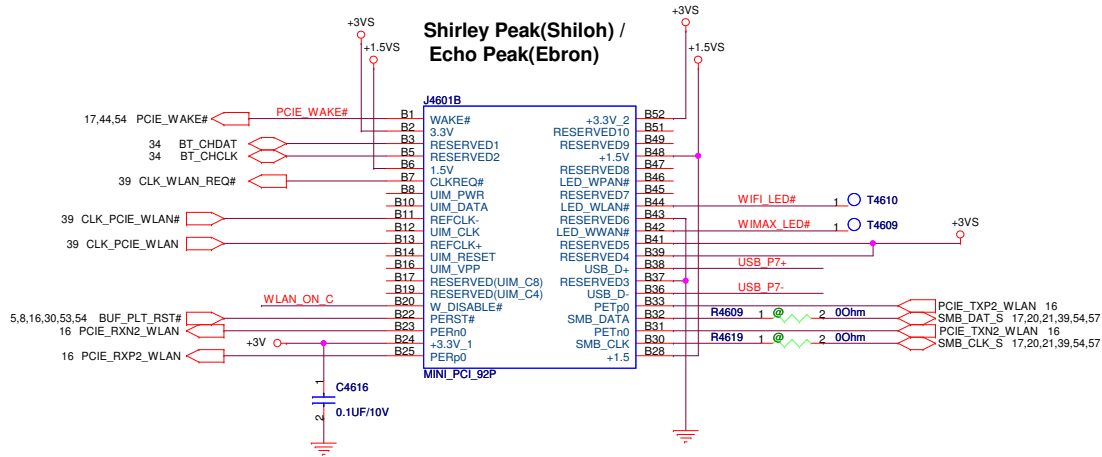


LAN CONN.

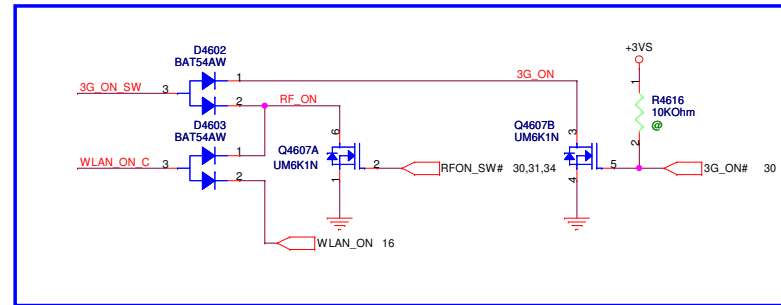
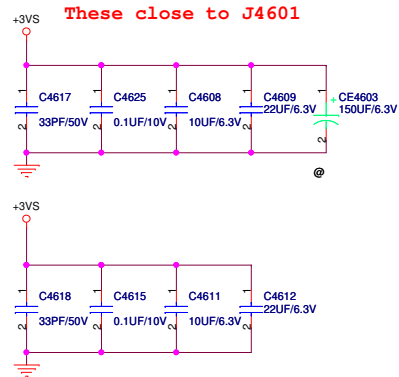




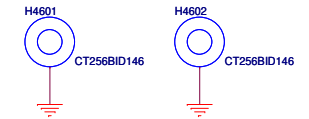
Shirley Peak(Shiloh) / Echo Peak(Ebron)



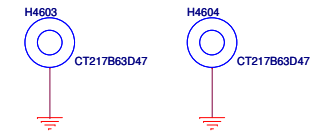
These close to J4601



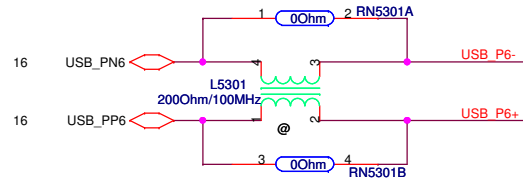
H=2+1



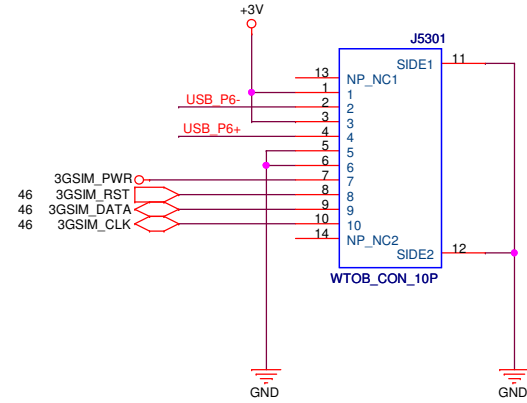
H=7.5mm



<Variant Name>

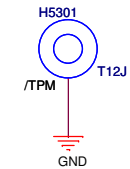
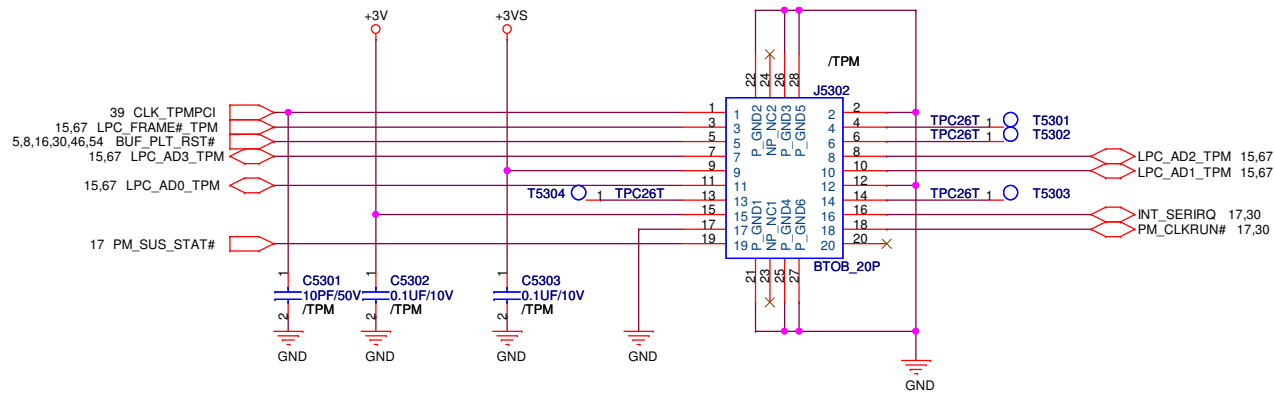


R1.1 081103-1



R1.1 081103-1

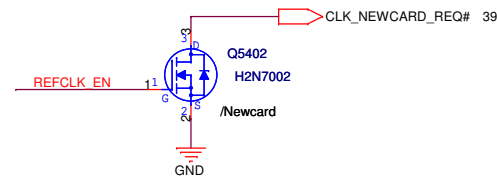
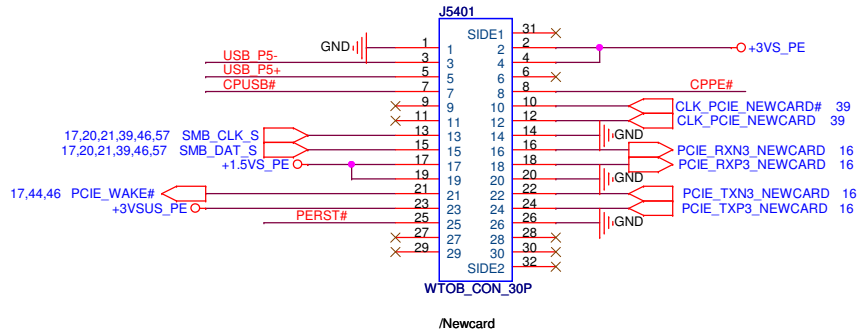
TPM Module CON

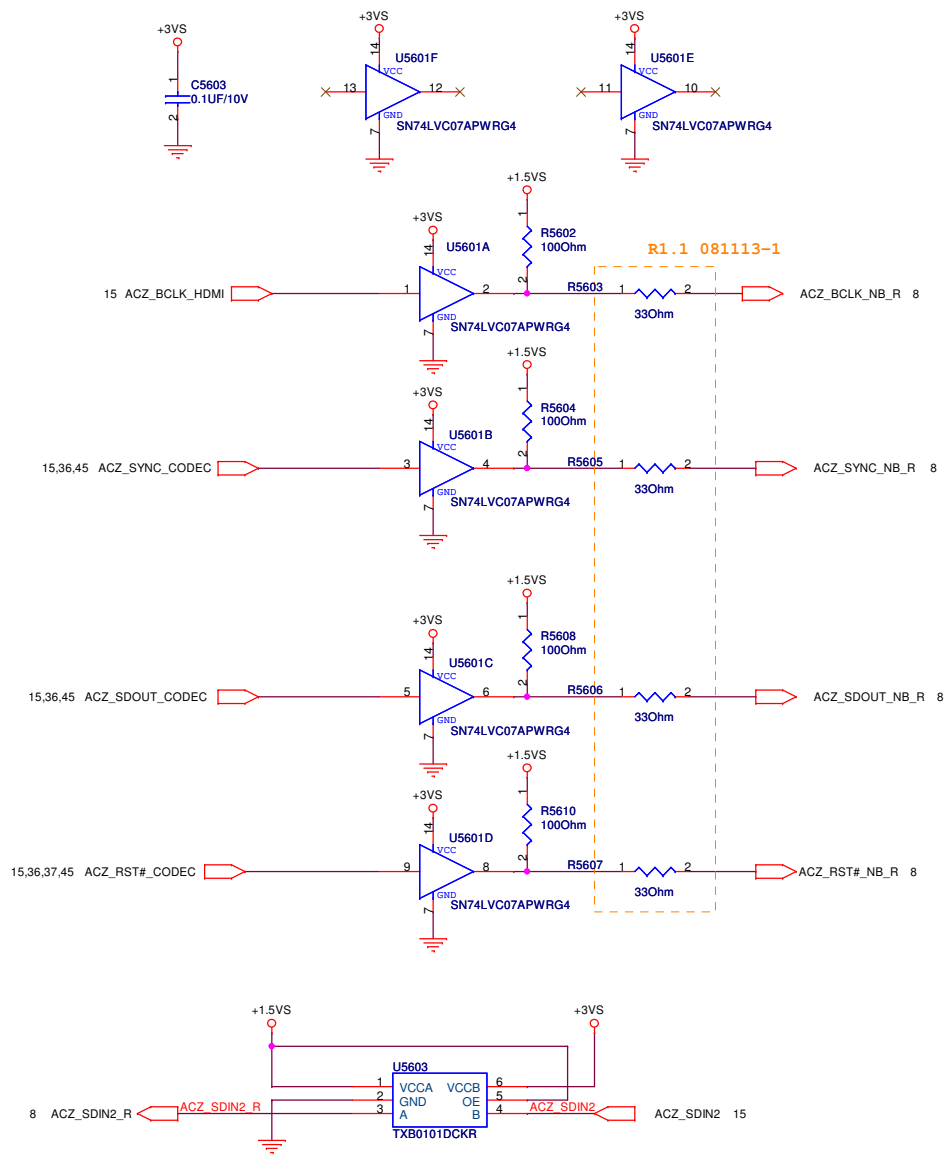


<Variant Name>

ASUS		Title: CardReader & SIM&TPM	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size B	Project Name F82		Rev 1.2
Date: Tuesday, December 30, 2008		Sheet 53 of 93	

NewCard Connector

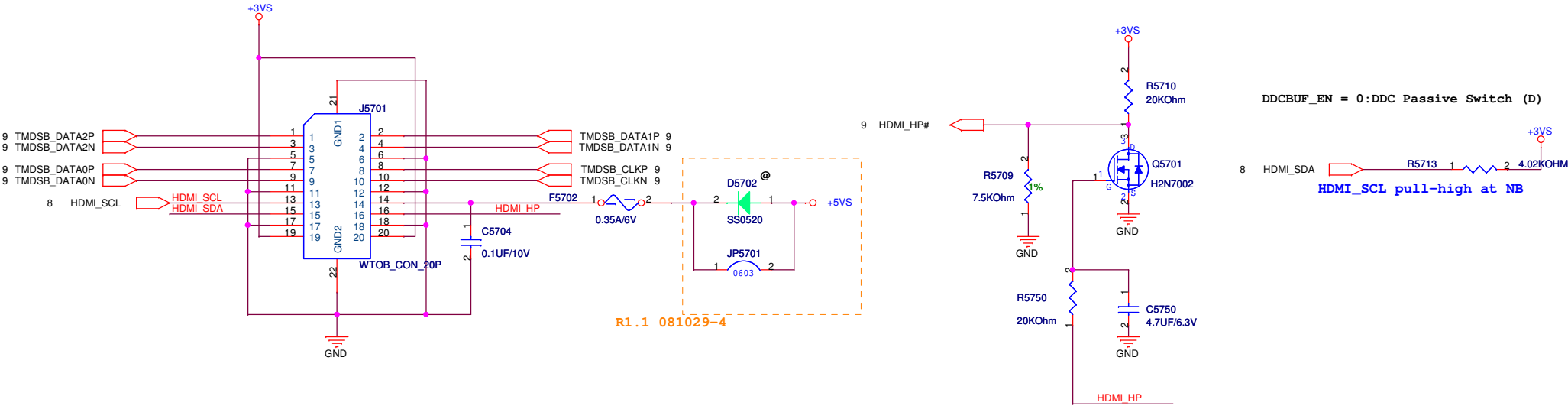




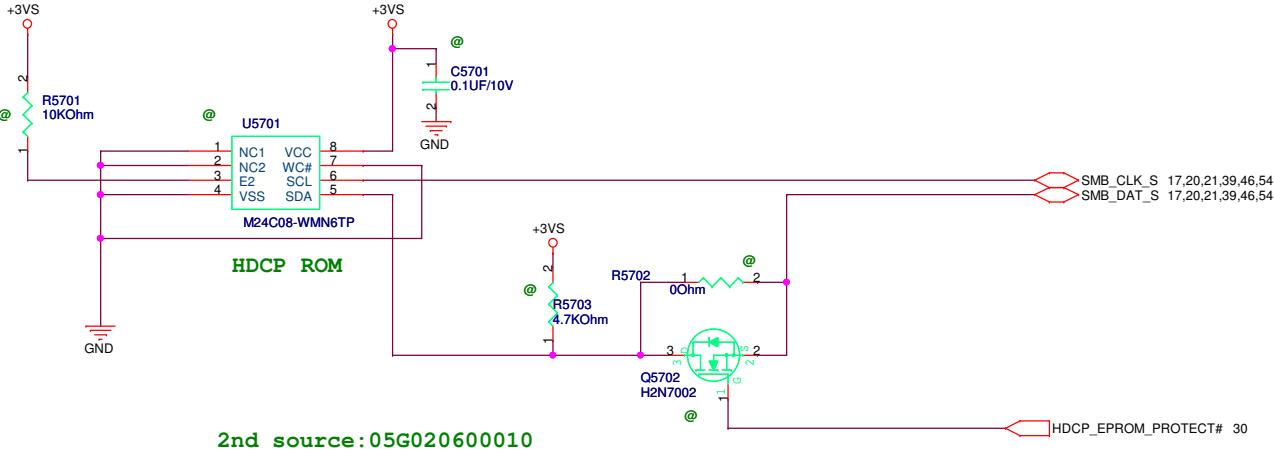
<Variant Name>

ASUS		Title : HDA level shifter	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size Custom	Project Name F82		Rev 1.2
Date: Tuesday, December 30, 2008		Sheet	56 of 93

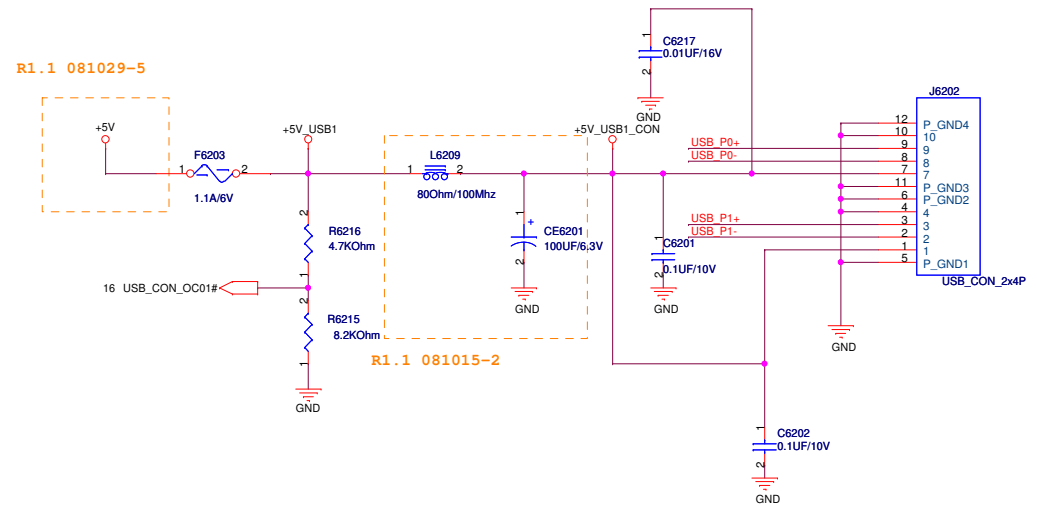
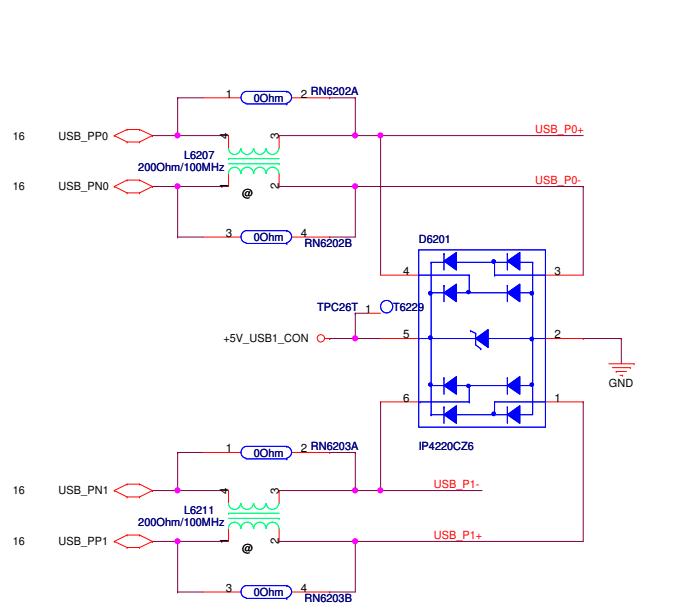
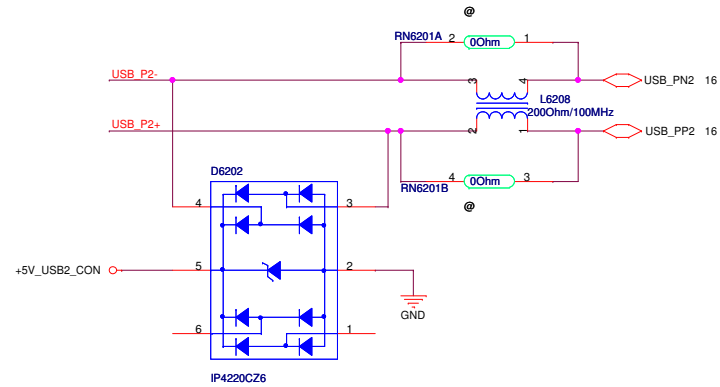
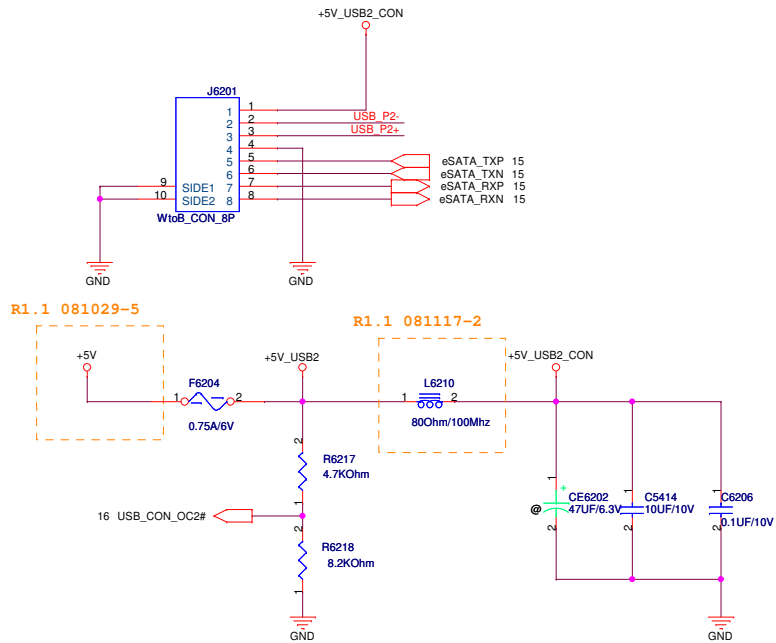
HDMI WtoB Connector



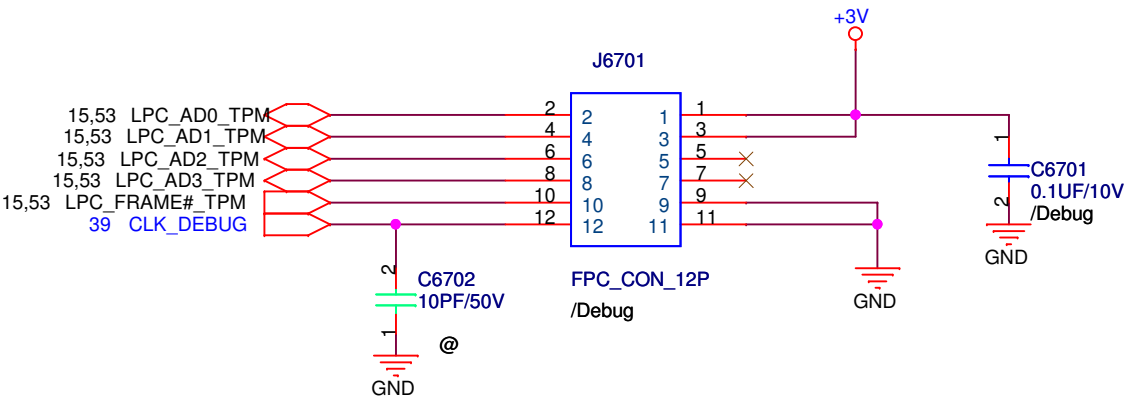
HDCEP ROM




USB IO Board



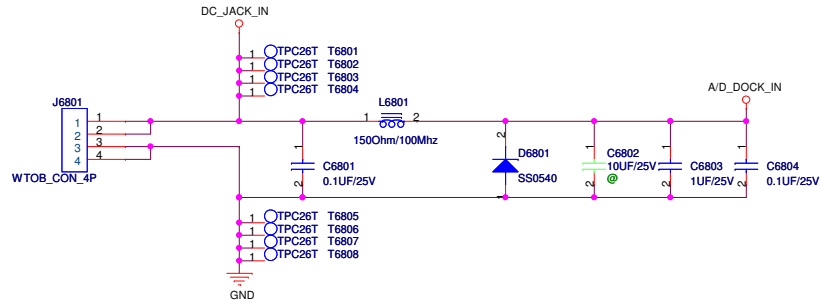
LPC DEBUG PORT



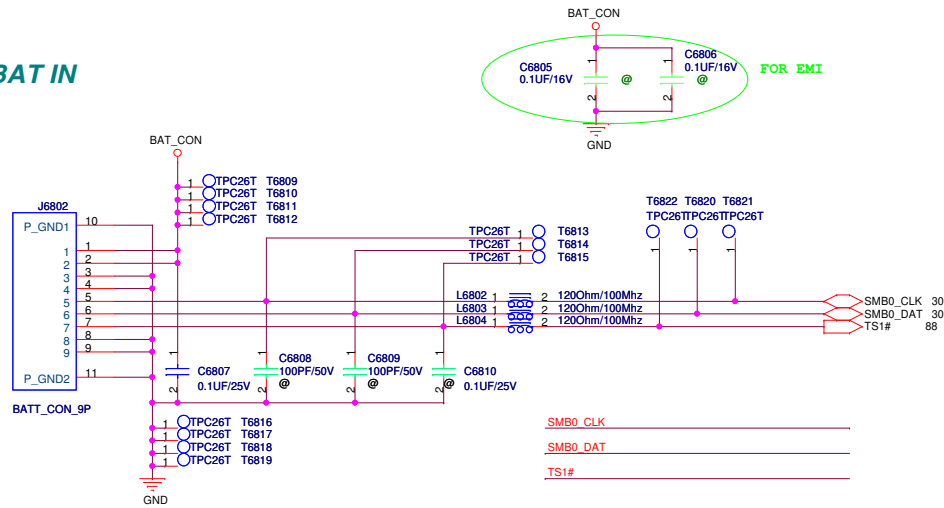
<Variant Name>

		Title : DEBUG CONN	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size A	Project Name F82		Rev 1.2
Date: Tuesday, December 30, 2008		Sheet 67 of 93	

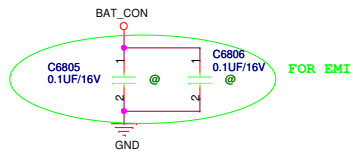
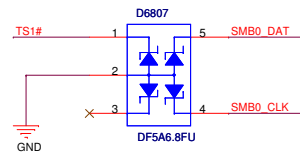
DC IN



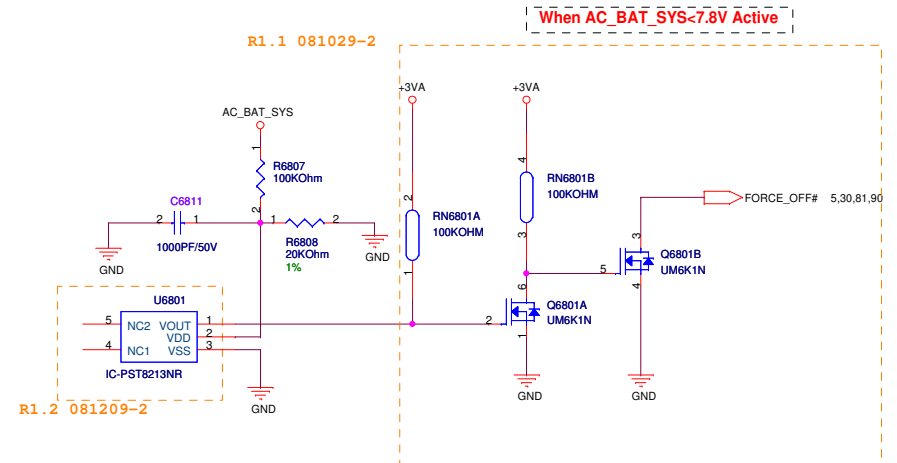
BAT IN



Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.



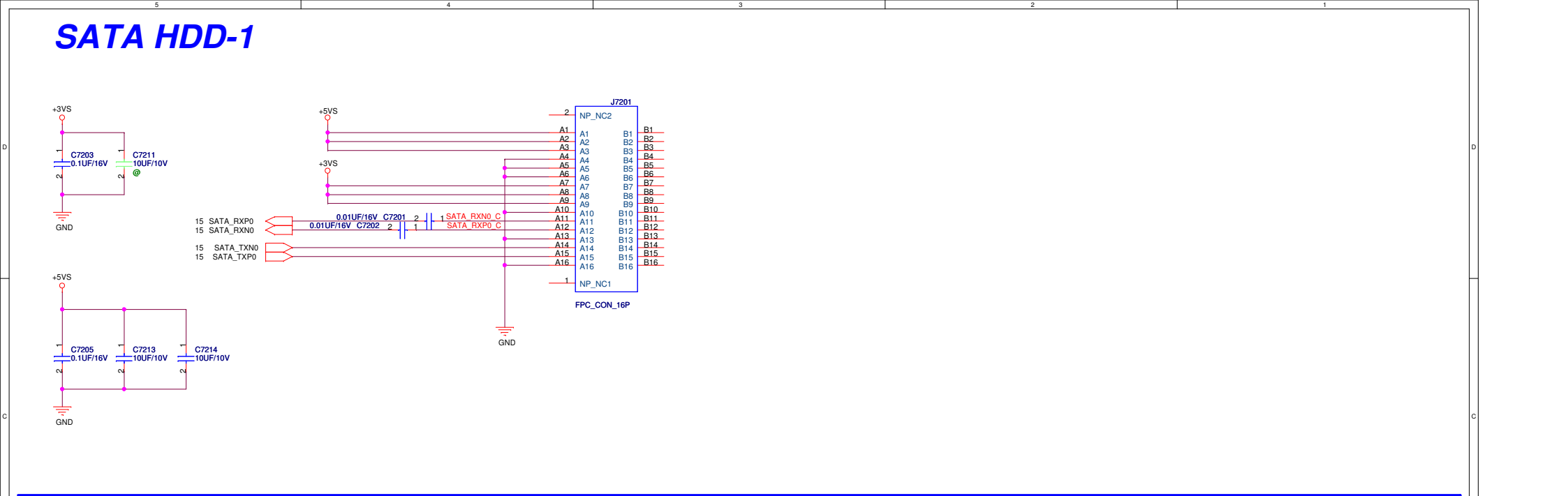
Without Battery & Pull out Adapter



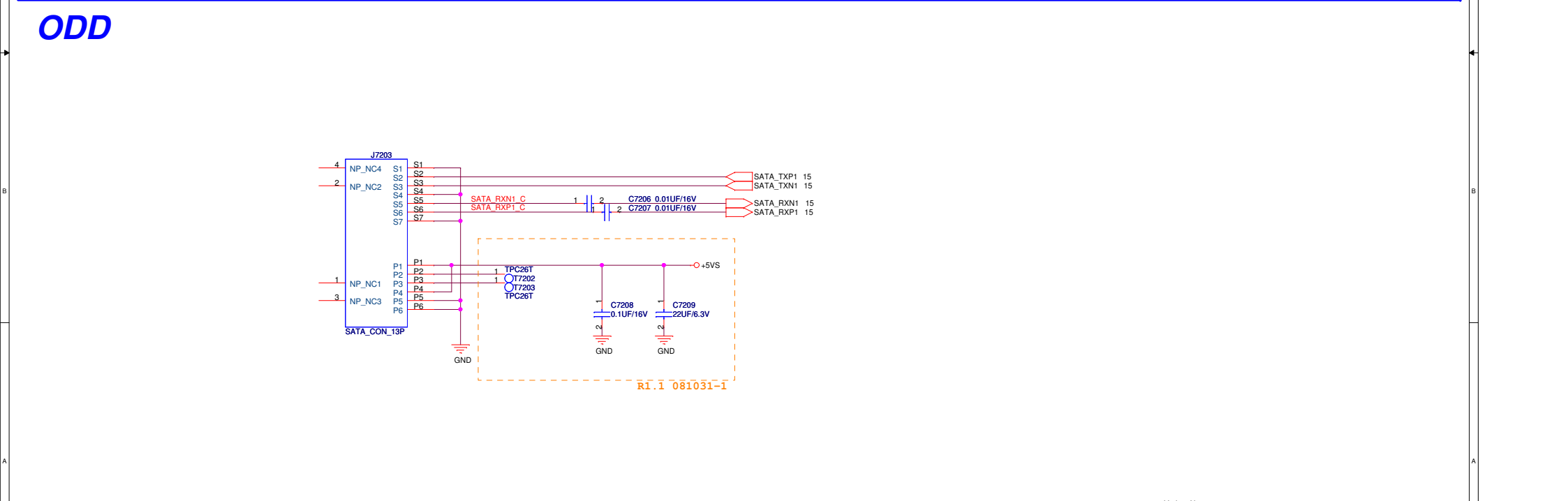
<Variant Name>

ASUS		Title : DC & BAT IN	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	F82	1.2	
Date: Tuesday, December 30, 2008		Sheet	68 of 93

SATA HDD-1



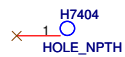
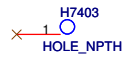
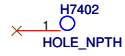
ODD



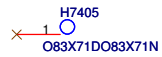
Hole-A



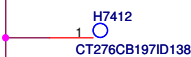
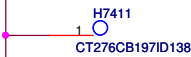
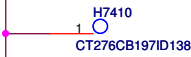
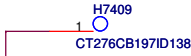
Hole-B



Hole-C

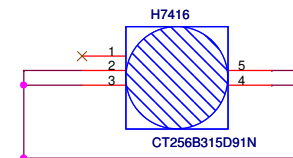
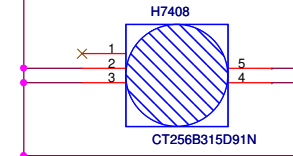
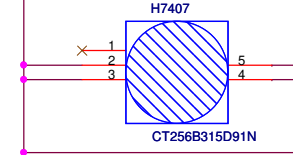
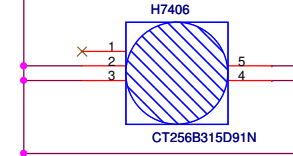
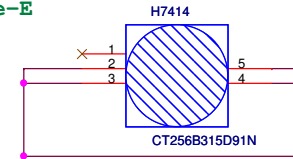


Hole-D



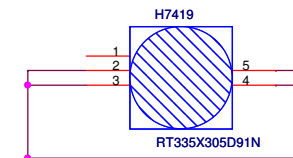
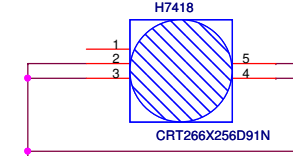
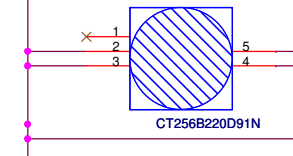
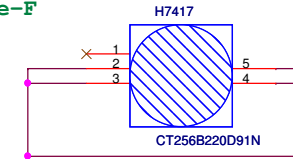
GND

Hole-E

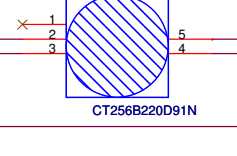
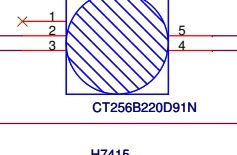
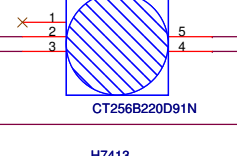
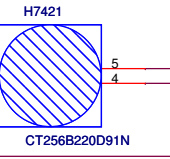


GND_AUDIO

Hole-F

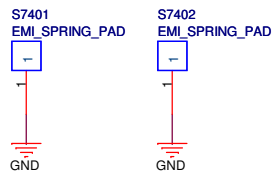


GND



GND

Spring



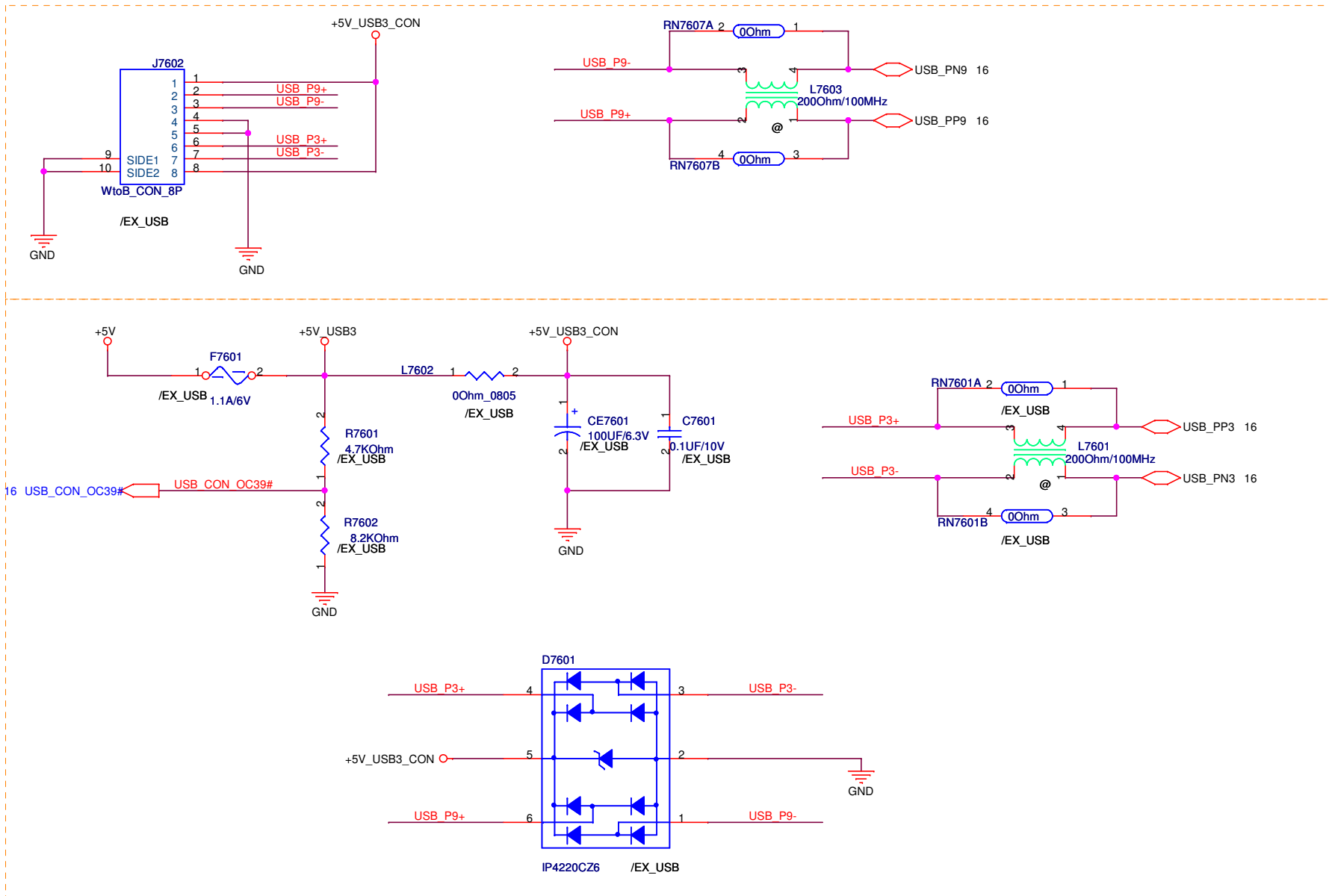
GND

GND

<Variant Name>

		Title : Hole	
ASUSTeK COMPUTER INC		Engineer: Leon Guo	
Size B	Project Name F82		Rev 1.2
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EXPRESS GATE CONN R1.1 081015-1



<Variant Name>

ASUS		Title :EX_USB*2	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	F82		1.2
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54321

R1.1 081015-1Reserve USB port on ExpressGate connectorpage16/76

R1.1 081015-2Move CE6201 after bead(L6209)page62

R1.1 081021-1Change pin2 from +3VS to +3Vpage53

R1.1 081028-1Change +3VS to +3VA_ECPAGE30

R1.1 081029-1Reserve ESD diode for ADJ_BL_CONpage33

R1.1 081029-2Add Q6801 to improve discharge speed of FORCE_OFF#page68

R1.1 081029-3Add R1537 to separate AC2_BCLKpage15

R1.1 081029-4Add 0 ohm(R5704)page57

R1.1 081029-5Del USB power switchpage62

R1.1 081031-1Swap ODD power(pin number is disorder)page72

R1.1 081031-2Change +5VSUS to +3VSUS(Charge LED)page31

R1.1 081031-3Change CLK_ICHPCI from pin64 to pin9.(Can't stop by STP_PCI#)page39

R1.1 081031-4Add BT_LED to RF LEDpage34/41

R1.1 081105-1Del CHG_EN#,PRECHG,BATSEL_2P# / Add ISET_EC,VSET_ECpage30

R1.1 081106-1Change Switch for ME requestpage41

R1.1 081106-2Change MDC/Nut height to 5mm for ME requestpage45

R1.1 081106-4Reserve for dynamic change Vcorepage30

R1.1 081106-5Change link after R1723page17

R1.1 081106-6Reserve for power sequencepage17

R1.1 081111-1Del reserve common chorkpage62

R1.1 081113-1Add Damping Rpage56

R1.1 081113-2Cost down, change LVDS connector to 30pinpage33

R1.1 081114-1Del PM_EXTTTS#_0 connected to DDR slotpage08/15

R1.1 081114-2For EMI requestpage20

R1.1 081117-1Add R0501 & R0502 for ATSpage5

R1.1 081117-2Add L6201 for EMI requestpage62

R1.1 081117-3Add C3808 for EMI requestpage38

R1.1 081118-1Change 83nH to 47nHpage32

R1.1 081118-2Reserve Cap for EMI requestpage17/33

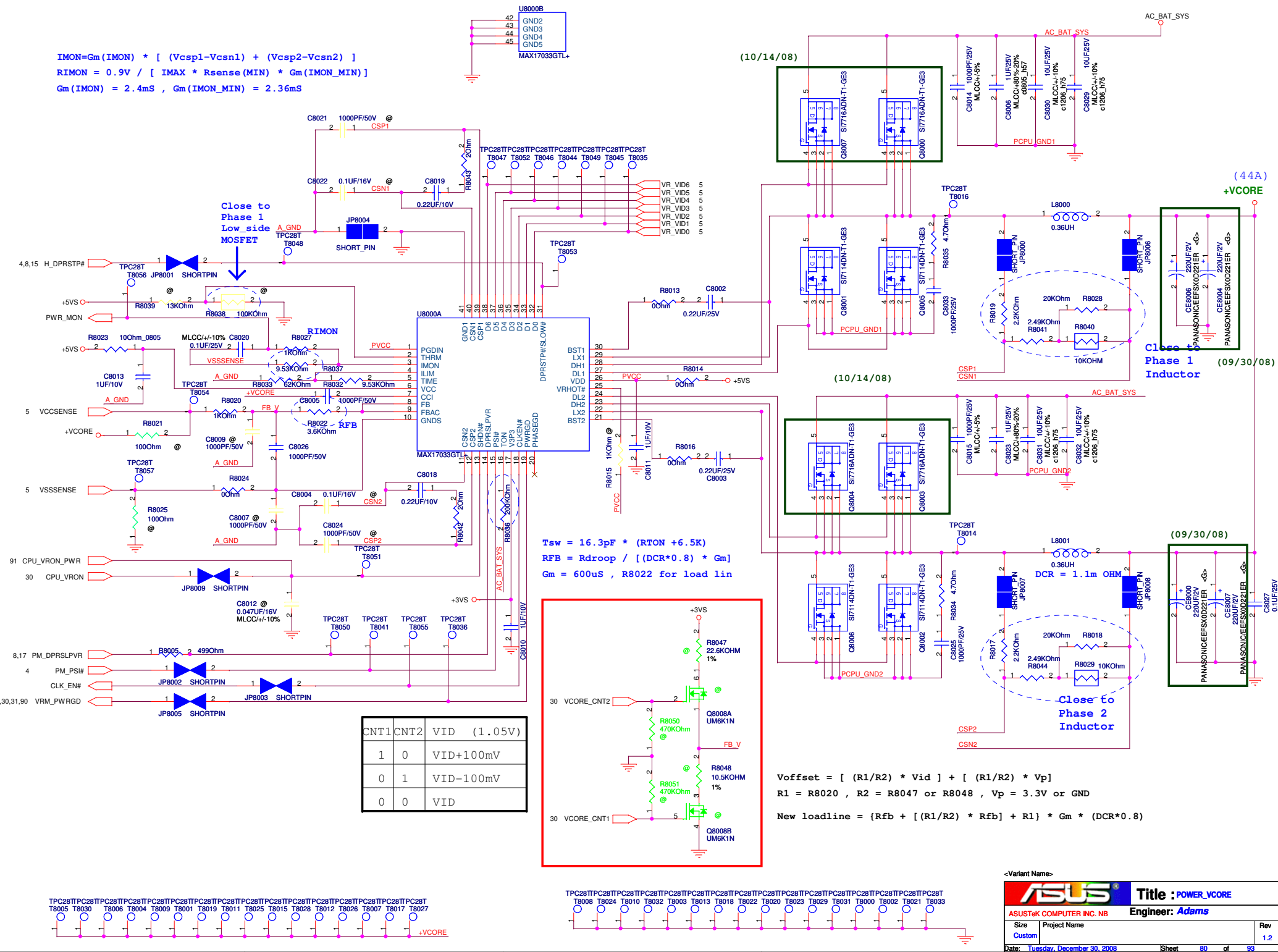
R1.2 081202-1Change to 40 pin connecotor and add 2nd LVDSpage09/33

R1.2 081209-1Add Buffer on HSYNC/VSYNCPAGE32

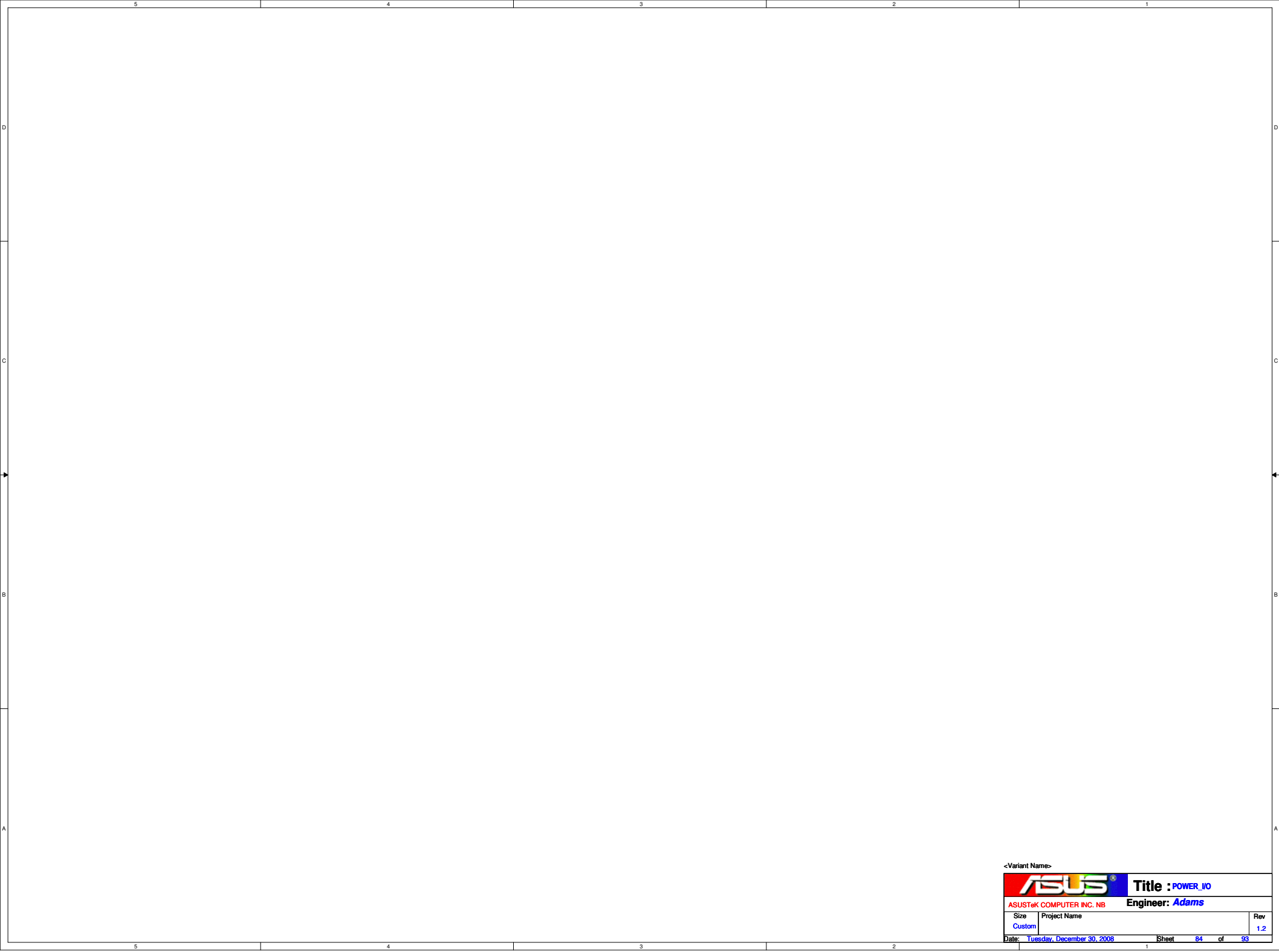
R1.2 081209-2Change Reset IC to new versionpage68

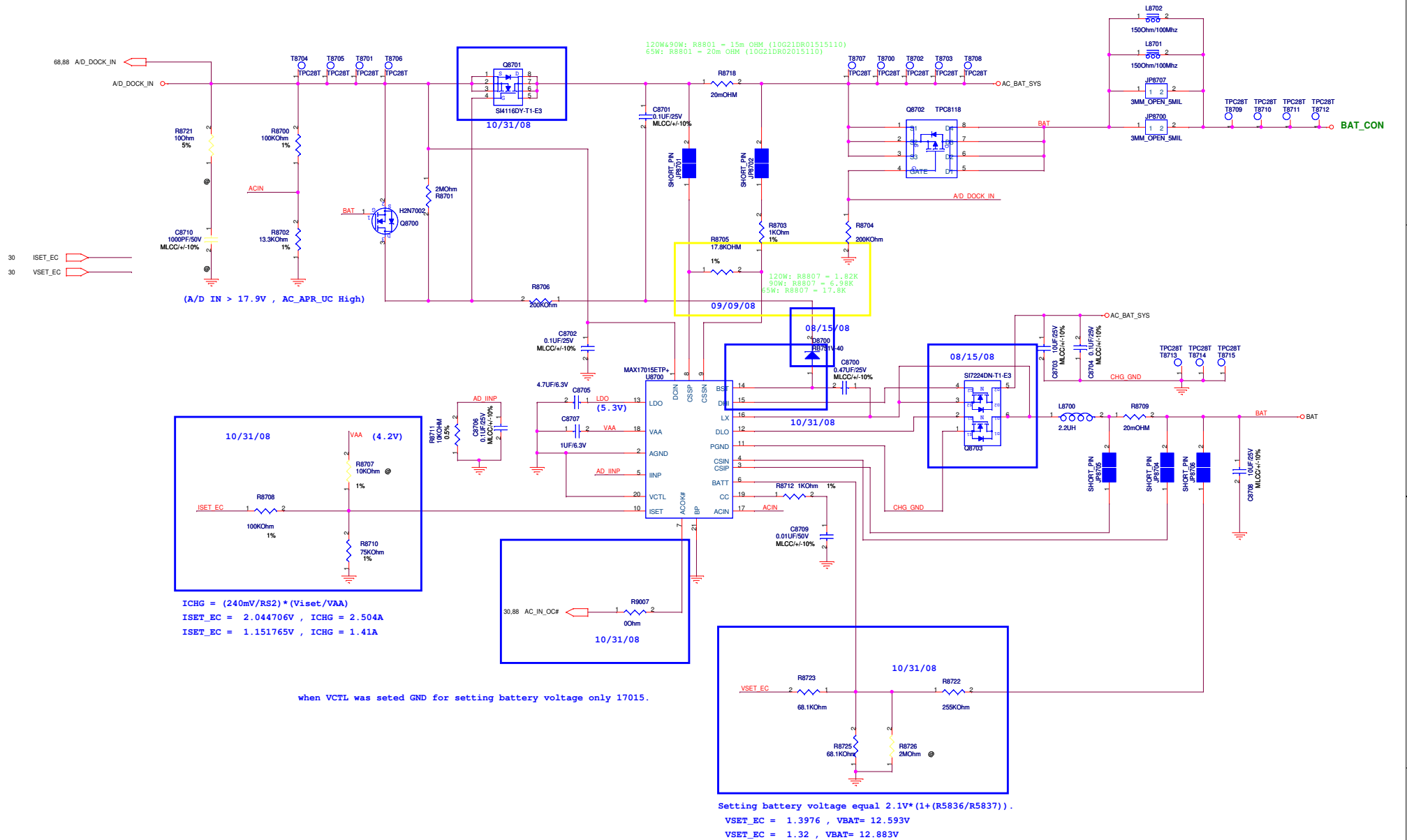
R1.2 081217-1Change LAN_DISABLE from pin35 to pin118 of ECpage30

$IMON = Gm(IMON) * [(Vcspl - Vcsn1) + (Vcsp2 - Vcsn2)]$
 $RIMON = 0.9V / [IMAX * Rsense(MIN) * Gm(IMON_MIN)]$
 $Gm(IMON) = 2.4mS, Gm(IMON_MIN) = 2.36mS$

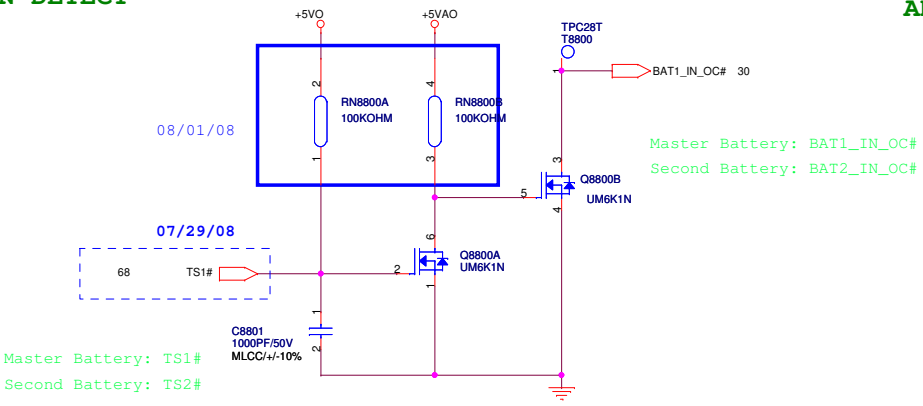


<Variant Name>

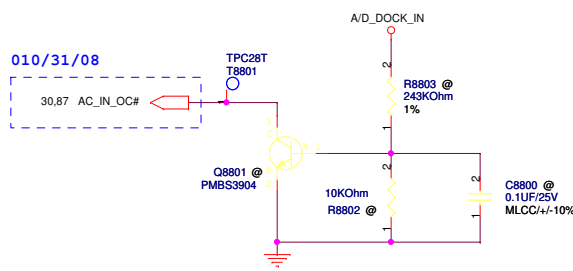




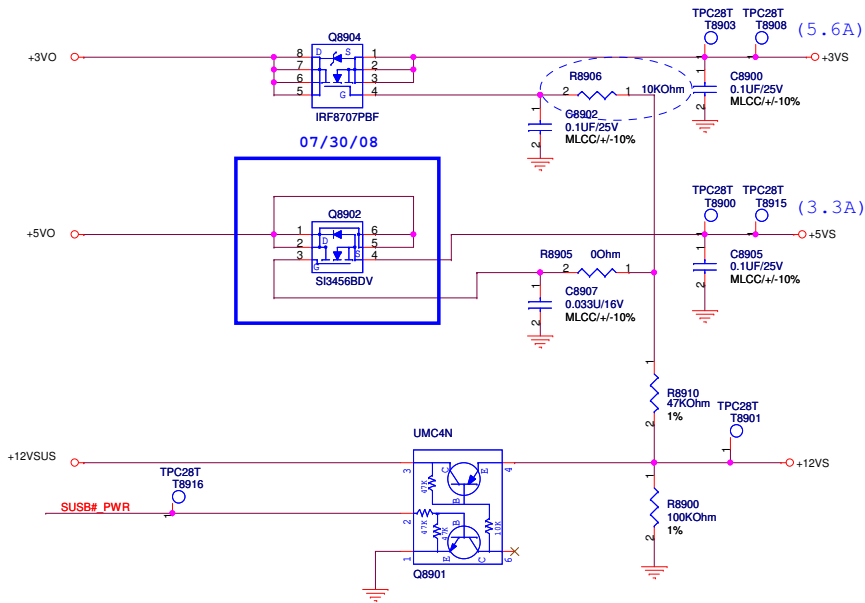
BATTERY IN DETECT



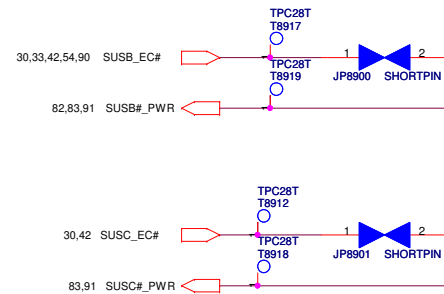
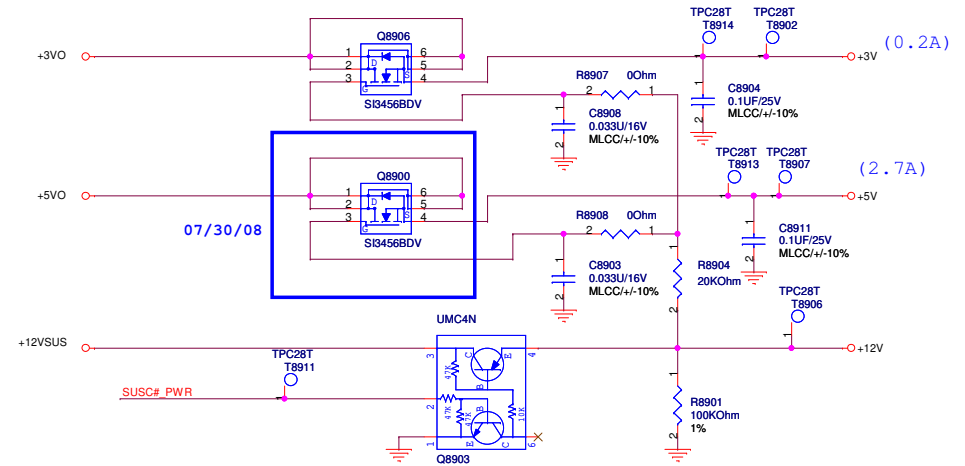
ADAPTER IN DETECT



SUSB#_PWR POWER



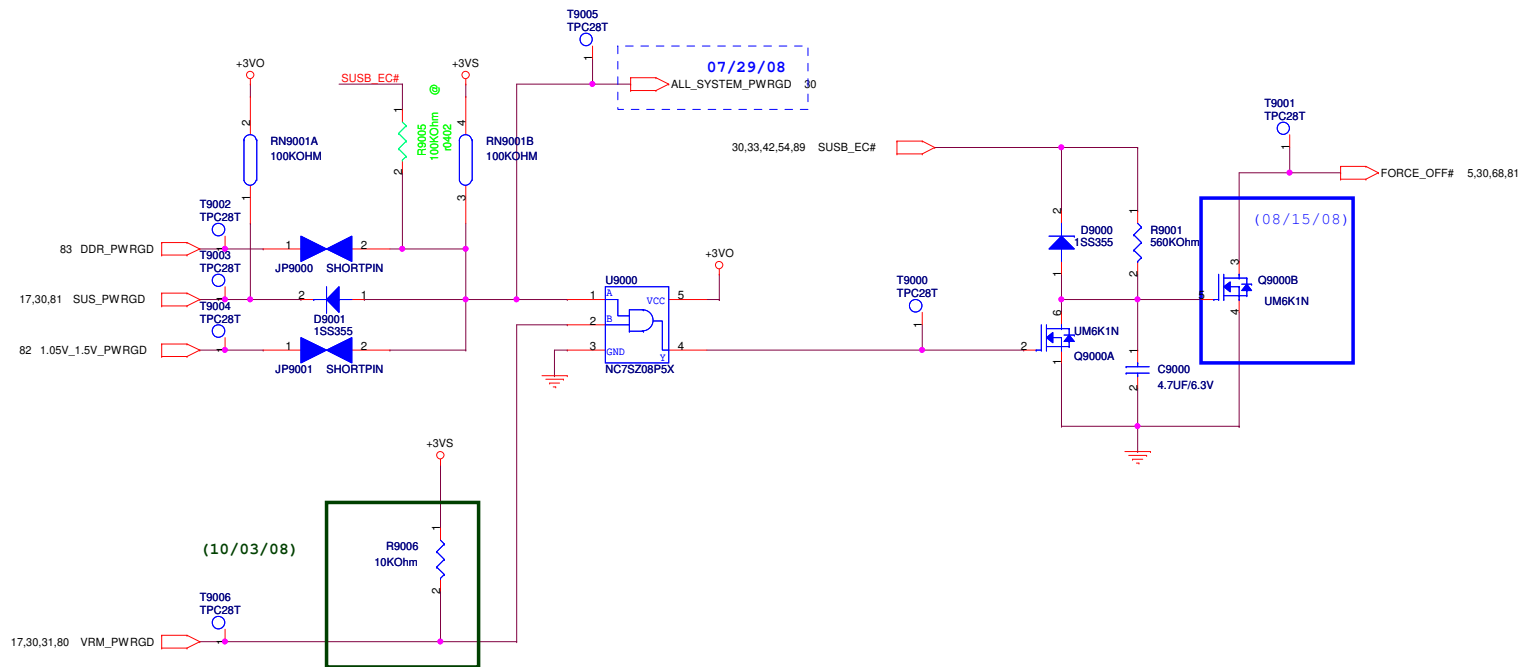
SUSC#_PWR POWER



<Variant Name>

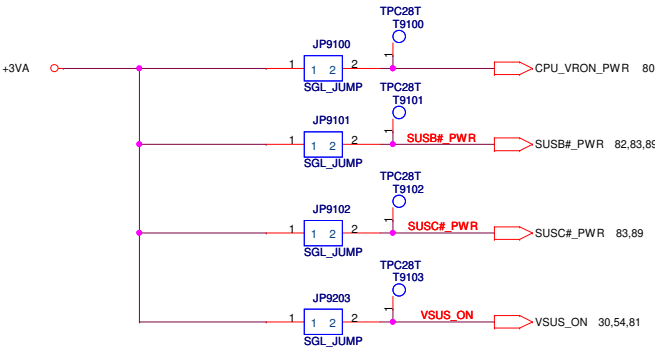
ASUS		Title : POWER LOADSWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: Adams	
Size	Project Name	Rev	
Custom		1.2	
Date: Tuesday, December 30, 2008		Sheet	89 of 93

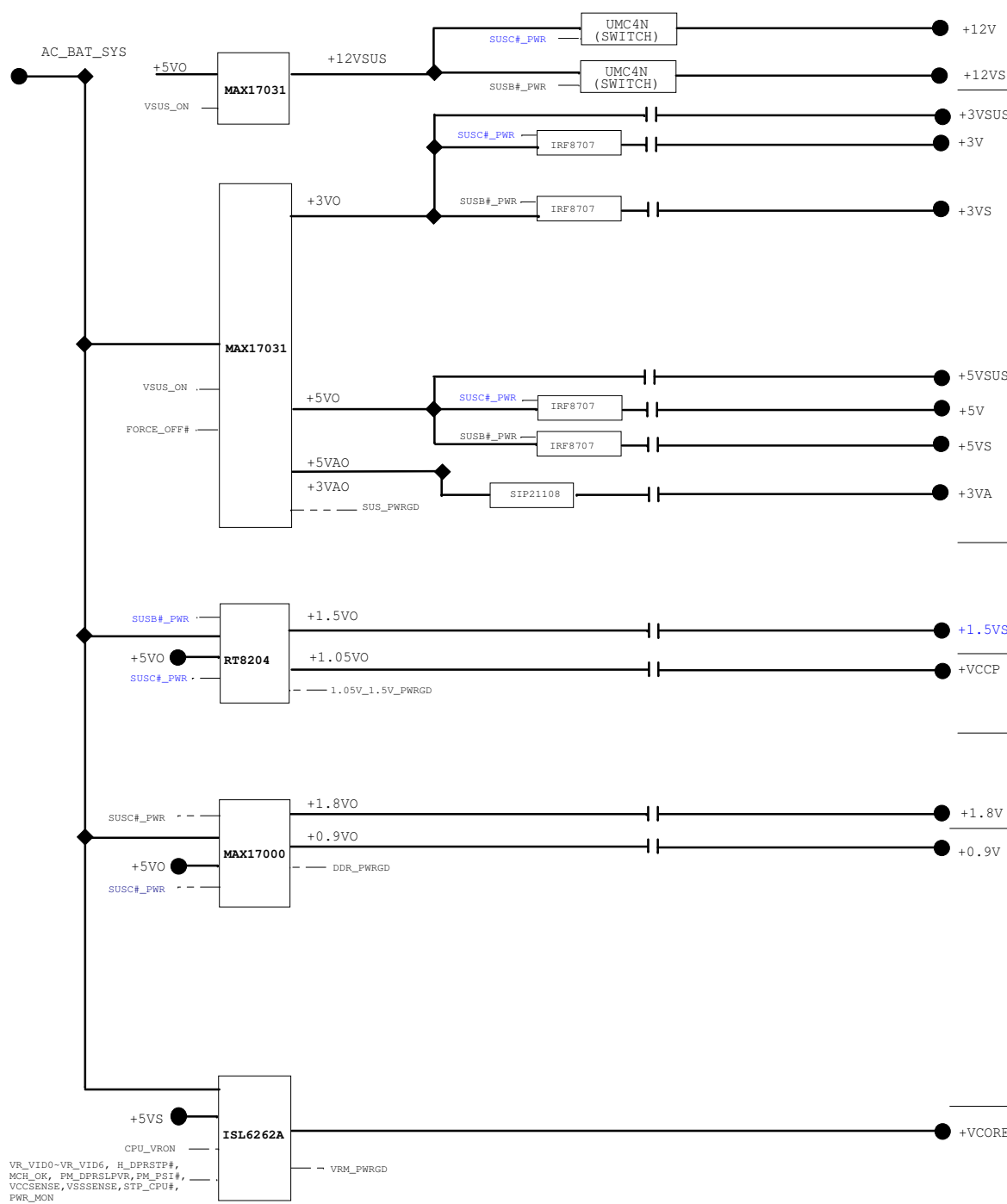
POWER GOOD DETECTOR



AC_BAT_SYS		AC_BAT_SYS	31,33,68,80,81,82,83,87
BAT		BAT	87
BAT_CON		BAT_CON	68,87
+3VAO		+3VAO	81
+3VA		+3VA	15,30,33,42,68,81
+5VAO		+5VAO	81,88
+5VO		+5VO	81,82,83,88,89
+3VO		+3VO	81,89,90
+1.8VO		+1.8VO	82,83
+0.9VO		+0.9VO	83
+1.05VO		+1.05VO	82
+1.5VO		+1.5VO	82
+5VSUS		+5VSUS	18,81
+5VSUS		+5VSUS	18,81
+3VSUS		+3VSUS	15,16,17,18,30,31,44,54,81
+12VSUS		+12VSUS	81,89
+5V		+5V	33,41,42,62,76,89
+3V		+3V	31,33,34,41,42,45,46,53,67,89
+12V		+12V	42,89
+1.8V		+1.8V	8,11,12,20,21,42,83
+0.9V		+0.9V	22,42,83
+3VS		+3VS	4,8,9,12,15,16,17,18,20,21,30,31,32,33,36,37,38,39,41,42,44,46,53,54,56,57,72,80,89,90
+5VS		+5VS	17,18,31,32,36,38,42,57,72,80,89
+12VS		+12VS	33,42,89
+1.5VS		+1.5VS	5,12,18,42,46,54,56,82
+VCCP		+VCCP	4,5,7,8,9,11,12,15,18,39,42,82
+VCORE		+VCORE	5,80

FOR POWER TEST





Spec rating	Design rating
(10mA)	
(10mA)	
(1.04A)	OCP Setting 7.2A
(0.3A)	
(5.6A)	
(0.03A)	OCP Setting 7.2A
(2.7A)	
(3.3A)	
(0.02A)	
(3.5A)	OCP Setting 5A
(10A)	OCP Setting 12A
(8A)	OCP Setting 9.6A
(1A)	(2A)
(44A)	

(08/15/08)

1. Q8706B rename to Q8704B .
2. Q9002 rename to Q8703 .
3. Q8203 rename to R8209 .
4. U8000 change from ISL6262A to ISL6266A .
5. Change R8015 from 255 OHM to 100 OHM.
6. Change C8004 from 470p to 270p.
7. Change C8011 from 1000p to 2200p.
8. Change C8013 from 220p to 100p.
9. Q9001B rename to Q9000B .
10. Change D8700 from 1SS355 to RB751
11. Unmount R8708 (Battery pack have pre-charge function)

(08/19/08)

12. Delete 1.5VSUS circuit .
13. Q8802A rename to Q8800A .
14. Add L8000,L8001 FB short pin .

(08/26/08)

15. Fix RT8204(U8200) to PWM mode .
16. Unmount R8715 .
17. Change R8208 to 4.02K ,R8205 to 10K .

(08/29/08)

18. Change U8200 PCB footprint .

(09/01/08) 243 pcs

19. Change Vcore solution to MAX17033 .

(09/02/08) 241 pcs

20. Delete R8102,R8103, connect U8100 pin 2 to pin 4 .
21. Add R8720 10HM .

(09/09/08) 242 pcs

22. Add D8701 , unmount .

R1.1 -- (09/30/08)

23. Change L8300 to 1.5uH
24. Change R8200 to 9.09K
25. Change CE8000,8004,8006,8007 to 220uF/2V/9mOHM
26. Change U8101 to MIC5378
27. Change R8111 to 232K

28. 3V_5V_PWRGD rename to SUS_PWRGD
29. Change R9001 to 4P2R , add R9006 .

(10/14/08)

30. Change Q8000,8003,8004,8007 to SI7716ADN

(10/21/08)

31. Del D8701 .
32. Modify circuit : Charge Vset & Iset control from EC .
33. Change Q8707 to SI4116 .

(12/10/08)

34. Add C8215 for LDO transient .

05/26

PEGATRON		Title :POWER_HISTORY	
ASUSTeK COMPUTER INC. NB		Engineer: Wit_Yang	
Size	Project Name		Rev
C	F82		1.2
Date: Tuesday, December 30, 2008		Sheet	83 of 83